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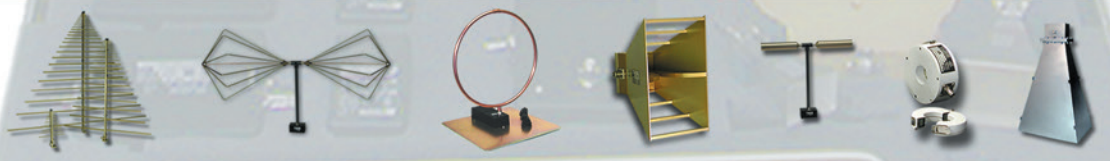

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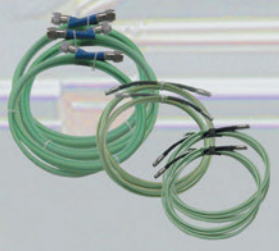

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Volume 12 | Number 9

FCC Levies $2.8 Million Fine for Illegal Drone Transmitters

The FCC received multiple complaints against HobbyKing regarding marketing of the illegal transmitters

In a case dating back more than four years, the U.S. Federal Communications Commission (FCC) has ordered retailer HobbyKing to pay a nearly $2.9 million fine in connection with the company's marketing of drone transmitters that operated in unauthorized radio frequency bands.

According to a Forfeiture Order issued by the FCC in late July, the company "advertised and sold on its website to U.S. consumers dozens of models of auto/video transmitters for use with unmanned aircraft systems (drones), without regard to whether those AV transmitters were compliant with the…Commission's rules."

The devices reportedly provide a video link between transmitters mounted on drones and drone users but can operate outside of frequency bands designated for amateur use, thereby requiring FCC certification.

The FCC's Spectrum Enforcement Division initially investigated HobbyKing in 2016 after receiving multiple complaints regarding the company's marketing of the illegal transmitters. Subsequent investigations by the FCC determined that HobbyKing marketed at least 65 different transmitter models that had not been FCC certified.

More troubling, 12 of the models marketed by the company operated in restricted frequency reserved for federal uses and could interfere with critical systems of the Federal Aviation Administration (FAA) and other operations. In addition, three of the models were found to operate at power levels exceeding Commission limits, and that could interfere with FAA terminal doppler weather radar.

In its Forfeiture Order, the FCC cited HobbyKing for "persistently violating" the Commission's rules and for failing to respond to the Commission's orders in its investigation of the company's practices.

Boeing 737 Engine Covers May Be Susceptible to EMFs

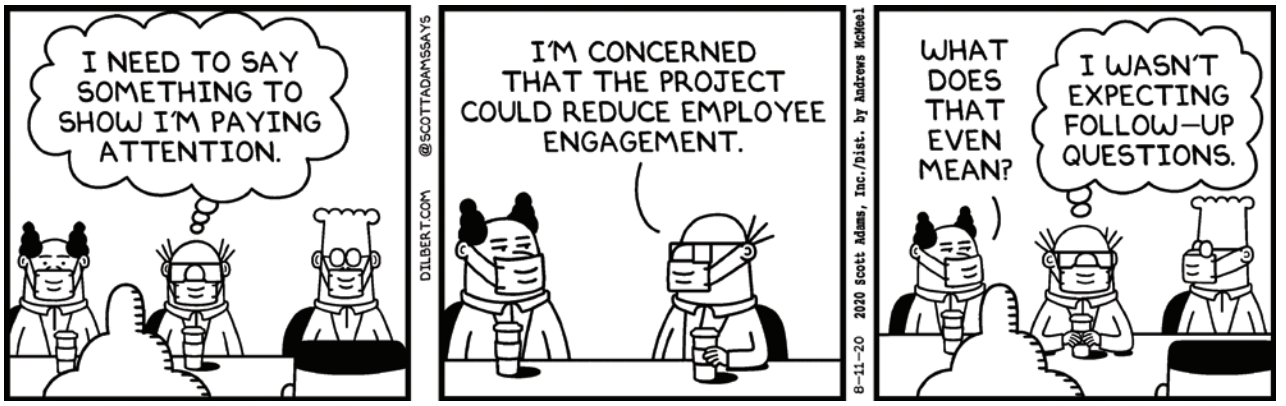
Inspections of the engine coverings will be required before the aircraft are cleared to fly

Safety officials at the U.S. Federal Aviation Administration (FAA) will require that airline manufacturer Boeing conduct inspections of engine coverings of its 737 MAX aircraft due to their potential vulnerability to electromagnetic fields (EMFs).

According to reported posted to the Brinkwire website, inspections of the engine coverings, also known as nacelles, will be required prior to the FAA providing Boeing with clearance to fly the 737 MAX aircraft. While the company successfully argued that the coverings provided a sufficient defense against lighting strikes, the FAA believes that "strong electromagnetic fields could cause a loss of power or faulty readings in the cockpit because of inadequate shielding around wiring."

Reportedly, routine polishing of the engine covering panels results in the loss of some layers of metal foil needed to properly shield internal wiring. Should the inspections find engine covering panels that have been "excessively reworked," the company will need to replace them prior to clearance.

Boeing's 737 MAX aircraft have been grounded since March 2019 following two separate crashes in 2018 and 2019 that claimed more 346 lives.



FCC Rule Strengthens Wireless 911 Location Accuracy Requirements

The U.S. Federal Communications Commission (FCC) has taken steps to strengthen its Enhanced 911 (E911) rules, thereby helping first responders more quickly locate 911 callers in multi-story buildings and other tall complexes.

According to a Sixth Report and Order issued by the Commission in mid-July, the FCC has now affirmed the so-called z-axis location accuracy metric requirements for wireless service providers. The z-axis metric is a coordinate-based location measurement that establishes the vertical location of a wireless handset within 3 meters. Adopting the z-axis metric as a requirement will enable service providers to transmit more accurate information to 911 call centers on the location of wireless emergency calls originating from multi-story buildings.

Compliance with the z-axis requirements will be mandatory for wireless companies serving the top 25 and 50 U.S. wireless markets, as of April 2021 and April 2023, respectively.

FCC Designates 988 as National Suicide Prevention Hotline

Acknowledging that the rate of suicides in the U.S. has reached crisis levels, the U.S. Federal Communications Commission (FCC) has officially designated the three-digit number "988" as a nationally-available telephone number to access suicide prevention and mental health crisis counselors.

A Report and Order issued by the Commission in mid-July implements new rules that will require all telecommunications carriers and voice over Internet protocol (VOIP) service providers to direct all calls made to 988 to the National Suicide Prevention Lifeline, a national network of about 170 separate crisis centers across the country. Carriers and service providers have until July 16, 2022 to effect the automatic transfer of 988 calls.

According to the FCC, suicide has ranked as the 10th leading cause of death in the U.S. since 2008. More than 48,000 Americans died from suicide in 2018, the equivalent of about one death from suicide every 11 minutes.

PRINCIPLES OF SWITCHED-MODE POWER SUPPLY DESIGN FOR EMC PERFORMANCE

By Bogdan Adamczyk

This article discusses the basics of a step-down (buck) DC Switched-Mode Power Supply (SMPS). It should serve at an entry-level tutorial and a building step towards the more advanced designs.

BASIC SMPS TOPOLOGY

The main functional objective of the buck SMPS is to step down a DC signal, V_{IN}, to a lower DC value, V_{OUT}, as shown in Figure 1.

The first step in this process consists of creating a Pulse-Width Modulated (PWM) version of the DC input signal, as shown in Figure 2.

The output signal shown in Figure 2 is far from the desired output signal described in our objective. Namely: 1) it is a constant signal only when the transistor is ON, 2) its level, when the transistor is ON, is not lower than the input signal, and 3) it contains high harmonic content during the transition times, [1].

Let's address the third aspect by placing a low-pass *LC* filter on the output side of the circuit, as shown in Figure 3.

To reduce the unwanted power dissipation in the circuit, *RC* and *RL* filters are avoided, and the basic designs utilize a simple *LC* filter.

Let's assume that the transistor is OFF, there is no energy stored in the LC filter, and the output voltage is zero. When the transistor turns ON we have the

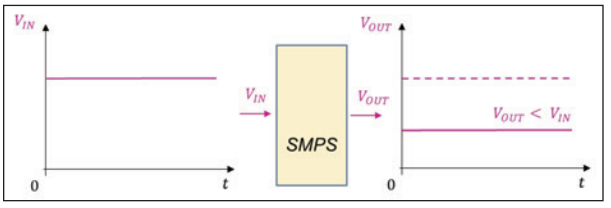


Figure 1: Objective of the buck SMPS

Dr. Bogdan Adamczyk is professor and director of the EMC Center at Grand Valley State University (http://www.gvsu.edu/emccenter) where he regularly teaches EMC certificate courses for industry. He is an iNARTE certified EMC Master Design Engineer. Prof. Adamczyk is the author of the textbook "Foundations of Electromagnetic Compatibility with Practical Applications" (Wiley, 2017) and the upcoming textbook "Principles of Electromagnetic Compatibility with Laboratory Exercises" (Wiley 2022). He can be reached at adamczyb@gvsu.edu.

circuit shown in Figure 4(a) (assuming an ideal transistor with no voltage drop).

The output voltage gradually increases. Assuming the ON time is long enough, this voltage eventually reaches the steady-state value $V_{OUT} = V_{IN}$. In steady-state the voltage across the inductor, v_L, is zero, and a dc current, I_L, flows through the inductor, as shown in Figure 4(b). The magnetic energy is stored in the inductor.

When the switch opens, a large negative voltage develops across the inductor and subsequently the switch. The magnetic energy stored in the inductor is

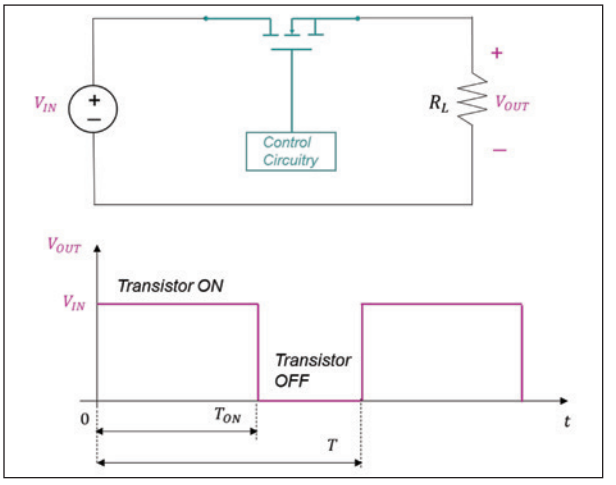


Figure 2: PWM signal

dissipated in the arc across the switch contacts or is radiated [2], as shown in Figure 5(a).

This behavior is often destructive to the switch, and some sort of a protective circuitry is required. The simplest solution is to provide a path for the inductor current during this switching event by inserting a diode in the circuit, as shown in Figure 5(b). We have arrived at one of the simplest step-down (buck) SMPS.

The basic design of this SMPS amounts to the proper choice of the components, L and C, to satisfy the imposed design requirements. The component values are determined through the circuit analysis when the transistor is ON (switch closed) and when it is OFF (switch open). The respective circuits and selected circuit variables are shown in Figure 6.

Note that in both cases, when the switch is closed and open, the inductor current is positive and flows in the same direction. If the switch remains open long enough the inductor current decays to zero and subsequently the output voltage goes to zero.

If the switch closes before the inductor current (and output voltage) goes to zero in the switching cycle, the SMPS will operate in the so-called *continuous conduction mode*. This is the preferred mode in EMC – it results in a smaller output ripple, smaller load-current variations, and lower EMC emissions.

When the switch subsequently opens, the output voltage rises. When it reaches the desired value, $V_{OUT} < V_{IN}$, the switch opens again. In a continuous mode and a steady-state operation, the inductor current and output voltage always stay positive and never go to zero.

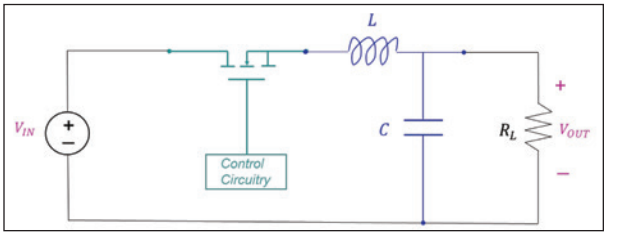


Figure 3: SMPS circuity with a low-pass filter

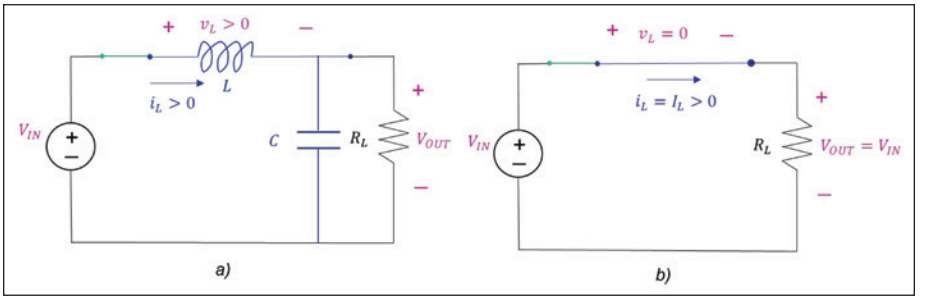


Figure 4: Transistor ON for the first time: a) transient behavior, b) steady-state

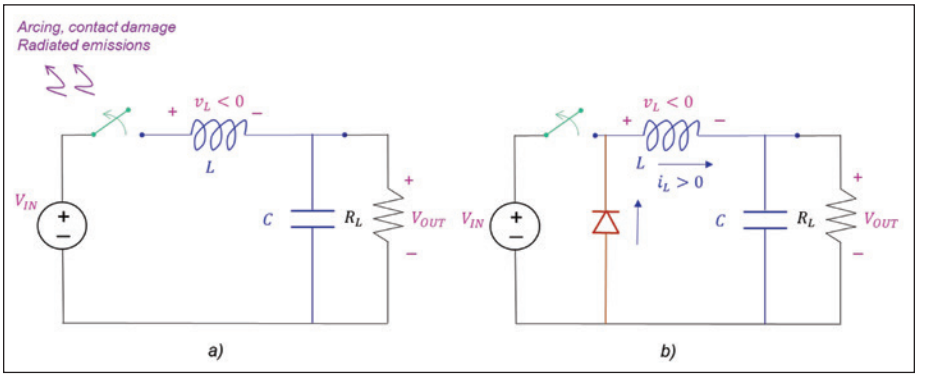


Figure 5: Transistor switches OFF: a) unwanted behavior b) protective diode

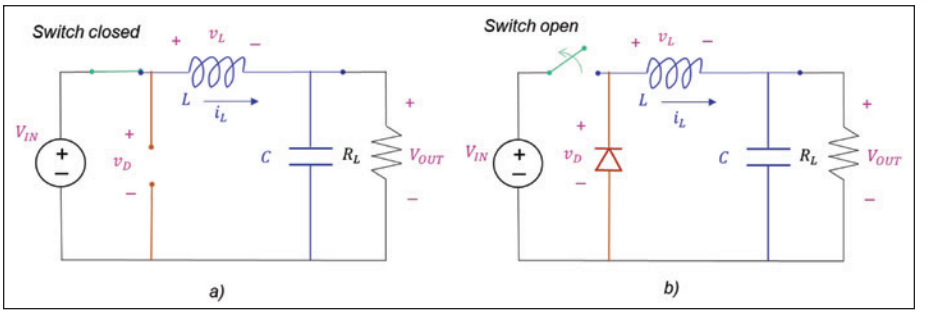


Figure 6: Step-down SMPS circuit: a) transistor ON b) transistor OFF

SMPS DESIGN

The following SMPS design assumes that the components are ideal – transistor and diode voltage drops are zero, inductor and capacitor are ideal (no parasitics). There are no losses in the circuitry – power supplied by the source equals the power delivered to the load. The approach discussed here is based on the material presented in [1].

The SMPS operates in a steady state, in a continuous conduction mode with the duty cycle, D, of the PWM signal equal to

$$D = \frac{T_{ON}}{T} = f_{SW} T_{ON} \tag{1}$$

where the switching frequency, f_{SW}, is constant. Switch is closed for time

$$T_{ON} = DT \tag{2a}$$

and is open for time

$$T_{OFF} = T - T_{ON} = T - DT = (1 - D)T \tag{2b}$$

When the switch is closed, the diode is reverse biased, and we have the circuit shown in Figure 7.

The voltage across the inductor is

$$v_L = L\frac{di_L}{dt} = V_{IN} - V_{OUT} \tag{3}$$

The voltage across the diode is equal to the input voltage, $v_D = V_{IN}$. From Eq. (3) we get

$$\frac{di_L}{dt} = \frac{V_{IN} - V_{OUT}}{L} > 0 \tag{4}$$

Since this derivative is positive, the inductor current increases linearly during the time when the switch is closed. To determine the (approximate) change in the inductor current during that time we approximate the derivative in Eq. (4) by

$$\frac{di_L}{dt} \cong \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT} = \frac{V_{IN} - V_{OUT}}{L} \tag{5}$$

Thus, the change in the inductor current is

$$(\Delta i_L)_{closed} = \left(\frac{V_{IN} - V_{OUT}}{L}\right) DT \tag{6}$$

When the switch is open, the diode is forward biased, ($v_D = 0$), and we have the circuit shown in Figure 8.

The voltage across the inductor is

$$v_L = L\frac{di_L}{dt} = -V_{OUT} \tag{7}$$

From Eq. (7) we get

$$\frac{di_L}{dt} = \frac{-V_{OUT}}{L} < 0 \tag{8}$$

Since this derivative is negative, the inductor current decreases linearly during the time when the switch is open. The (approximate) change in the inductor current during that time is obtained from

$$\frac{di_L}{dt} \cong \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{-V_{OUT}}{L} \tag{9}$$

Thus, the change in the inductor current is

$$(\Delta i_L)_{open} = -\left(\frac{V_{OUT}}{L}\right)(1 - D)T \tag{10}$$

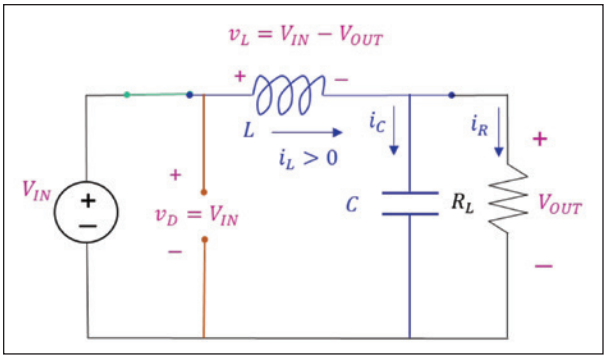


Figure 7: Circuit with the switch closed

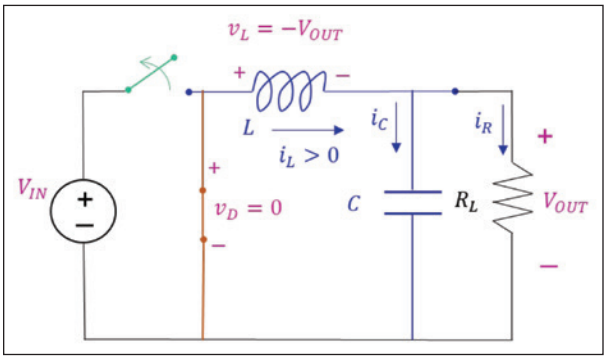


Figure 8: Circuit with the switch open

The variations in the inductor voltage and current are shown in Figure 9.

Obviously, $(\Delta i_L)_{closed} = \Delta i_L)_{open}$. From Eqs. (6) and (10) we get

$$\left(\frac{V_{IN}-V_{OUT}}{L}\right)DT = -\left(\frac{V_{OUT}}{L}\right)(1-D)T \tag{11}$$

or

$$(V_{IN}-V_{OUT})D = V_{OUT}(1-D) \tag{12}$$

resulting in an input-output relationship for a buck converter

$$V_{OUT} = DV_{IN} \tag{13}$$

Since the duty cycle is less than 1, the output voltage is lower than the input voltage. We can control the level of the output voltage by simply changing the duty cycle.

Next, let's calculate the average, maximum, and minimum inductor currents. In a steady-state operation the average capacitor current, $I_C = 0$, [3]. It follows that the average inductor current, I_L, must be the same as the average load current, I_R. That is,

$$I_L = I_R = \frac{V_{OUT}}{R_L} \tag{14}$$

From Figure 9, the minimum and maximum values of the inductor current are

$$I_{MIN} = I_L - \frac{|\Delta i_L|}{2} \tag{15a}$$

$$I_{MAX} = I_L + \frac{|\Delta i_L|}{2} \tag{15b}$$

Using Eqs. (10) and (14) in Eqs. (15) we get

$$I_{MIN} = \frac{V_{OUT}}{R_L} - \frac{1}{2}\left(\frac{V_{OUT}}{L}\right)(1-D)T \tag{16a}$$

$$I_{MAX} = \frac{V_{OUT}}{R_L} + \frac{1}{2}\left(\frac{V_{OUT}}{L}\right)(1-D)T \tag{16b}$$

or

$$I_{MIN} = V_{OUT}\left(\frac{1}{R_L} - \frac{1-D}{2Lf_{SW}}\right) \tag{17a}$$

$$I_{MAX} = V_{OUT}\left(\frac{1}{R_L} + \frac{1-D}{2Lf_{SW}}\right) \tag{17b}$$

where $f_{SW} = 1/T$.

Now, we can calculate the minimum value of the inductance, L_{MIN}, for the continuous mode of operation. At the boundary between the continuous and discontinuous mode $I_{MIN} = 0$. Thus, from Eq. (17a) we get

$$0 = V_{OUT}\left(\frac{1}{R_L} - \frac{1-D}{2L_{MIN}f_{SW}}\right) \tag{18}$$

or

$$L_{MIN} = \frac{(1-D)R_L}{2f_{SW}} \tag{19a}$$

or utilizing Eq. (13),

$$L_{MIN} = \frac{(V_{IN}-V_{OUT})R_L}{2f_{SW}V_{IN}} \tag{19b}$$

The actual value of the inductance should, of course, be larger than the minimum value given by Eqs. (19). A reasonable choice is

$$L = 1.25L_{MIN} \tag{20}$$

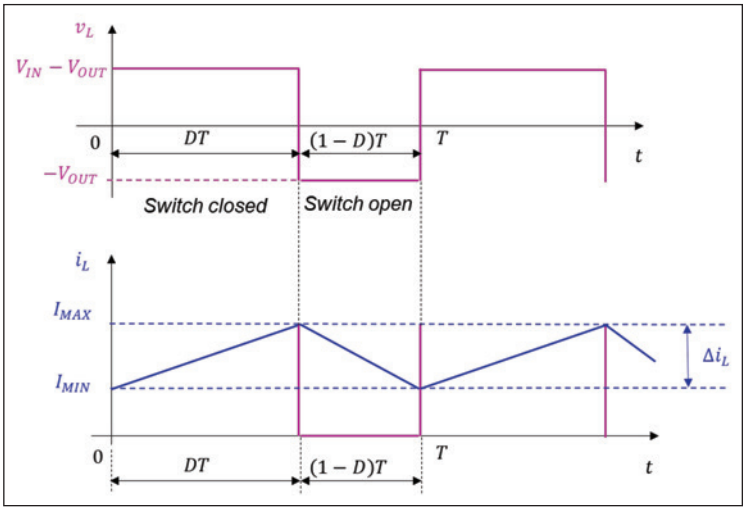


Figure 9: Variations in the inductor voltage and current

Finally, the output voltage ripple, ΔV_{OUT}, can be obtained by analyzing Figure 10, which shows the capacitor current and the output voltage curves, [1].

The change in the capacitor charge, ΔQ, is equal to the triangle area under the capacitor current curve when the capacitor is charging. That is,

$$\Delta Q = \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{\Delta i_L}{2}\right) \tag{21}$$

Since

$$C = \frac{Q}{V_{OUT}} \tag{22a}$$

it follows that

$$Q = CV_{OUT} \tag{22b}$$

and

$$\Delta Q = C\Delta V_{OUT} \tag{22c}$$

From Eq. (10),

$$\left|(\Delta i_L)_{open}\right| = \left(\frac{V_{OUT}}{L}\right)(1-D)T \tag{23}$$

Utilizing Eqs. (22c) and (23) in Eq. (21) we get

$$C\Delta V_{OUT} = \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{V_{OUT}}{2L}\right)(1-D)T \tag{24}$$

which leads to the output voltage ripple as

$$\Delta V_{OUT} = \frac{V_{OUT}(1-D)}{8LCf_{SW}^2} \tag{25}$$

The relative output voltage ripple is

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{1-D}{8LCf_{SW}^2} \tag{26}$$

which can be used to obtain the required capacitance in terms of the specified voltage ripple as

$$C = \frac{1-D}{8L(\Delta V_{OUT}/V_{OUT})f_{SW}^2} \tag{27}$$

In the design of a SMPS, the input and output voltages are usually specified. As are the load and the output voltage ripple. Once the switching frequency is chosen, the minimum inductor value can be calculated from Eq. (19b), and the capacitor value from Eq. (27).

This article presented the very basics of the simplest (and probably noisy) SMPS design. It should serve as an entry-level tutorial and a building step towards the more advanced SMPS. The next step in the design should include the non-ideal diode and transistor models, parasitics of the components and their physical limitations. To mitigate the EMC emissions, among many other considerations, an input filter [2] and a snubber circuitry [3,4] should also be implemented.

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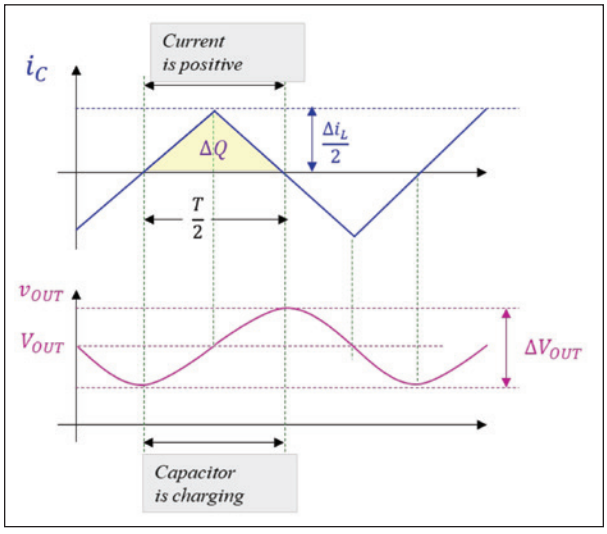

Figure 10: Variations in the capacitor current and output voltage

EVEN OPTICAL COMMUNICATION NEEDS ESD PROTECTION

By Bart Keppens for EOS/ESD Association, Inc.

In the past, fiber-optic communication was used primarily for long-distance communication (50 km and beyond). Only a limited number of these high-end interface products were required worldwide. More recently, companies running large data centers (Facebook, Google, Amazon) have been replacing the traditional copper cabling between server racks (Figure 1). The copper-based approach is considered a bottleneck for further improvements in data transfer capacity. Optical communication can dramatically increase the bandwidth between servers while reducing complexity, power consumption, and cost.

Bart Keppens received an engineering degree in electronics from Groep T, Leuven in 1996. Bart has co-authored more than 40 peer-reviewed published articles. He has been a member of the Technical Program Committee for the EOS/ESD Symposium since 2003. Bart holds several on-chip ESD protection design patents.

Founded in 1982, EOS/ESD Association, Inc. is a not for profit, professional organization, dedicated to education and furthering the technology Electrostatic Discharge (ESD) control and prevention. EOS/ESD Association, Inc. sponsors educational programs, develops ESD control and measurement standards, holds international technical symposiums, workshops, tutorials, and foster the exchange of technical information among its members and others.

REDUCING COST AND POWER WHILE INCREASING BANDWIDTH

Thus, the optical interconnect suppliers now need to produce a large number of their products. To reduce the cost, they separate the optical parts (laser diodes, photodetectors) from the digital controller circuits. For the electrical ICs, regular CMOS technology can be used for mass-production. Moreover, there were several technological breakthroughs in the last decade, where conventional CMOS processing steps facilitate the creation of several different optical components like WDM (Wavelength Division Multiplexers), lasers, detectors, waveguides in, e.g., SOI processes.

HYBRID 2.5D AND 3D INTEGRATION

Both optical and electrical elements are then combined within a single IC package using advanced packaging techniques like 2.5D (electronic interposer – Figure 2 on page 14) and 3D (flip-chip – Figure 3 on page 14) integration. The hybrid integration allows designers to select the best process option for each function; for example, the digital functions can be integrated in high-end CMOS technology with high performance and smaller size. The photonic die does not benefit from this minimum feature size and can thus be designed in a more mature SOI technology, which significantly reduces the total cost.

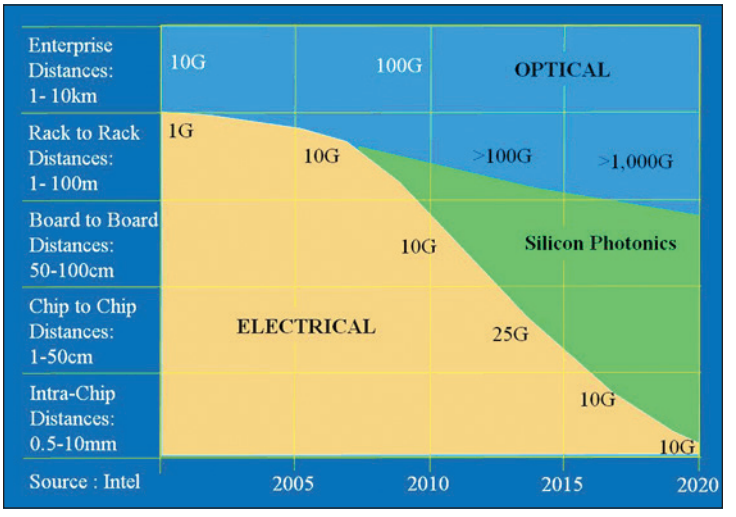

Figure 1: The engineers from the Intel groups working on optical communication summarized the potential for Silicon Photonics for different interface distances [1]. The traditional optical communication will be used mainly for the long distances. Silicon photonics will replace the electrical communication for the shorter distances thanks to the combination of low power, low cost, and high bandwidth opportunity.

OPTICAL LINKS NEED CUSTOM ESD CLAMPS

The electronic IC that is used to control the optical parts and to process the signals before transmitting or after receiving is manufactured using advanced CMOS technology like 28nm or below. The interfaces consist of high speed (25Gbps or higher) SerDes-type circuits.

To create such high-speed differential circuits, designers utilize the thin oxide transistors. However, those transistors are very sensitive and can be easily damaged during transient events like electrostatic discharge (ESD). The maximum voltage that these transistors can endure during transient events is 4V or less.

Even though the sensitive pads are not connected outside of the package, they could still receive ESD stress during assembly. Therefore, adequate protection clamps need to be inserted at the bond pads. On the other hand, for signal integrity, it is important to limit the capacitance between the interface pads and the supply lines. Selecting on-chip ESD protection with low parasitic capacitance has been studied by several authors in the past. Diode or SCR based protection concepts have been used for RF chips [4-8]. However, for the most sensitive interfaces running at low voltage, ESD protection based on dual diode at the I/O, combined with a (distributed) power clamp, is not always feasible [8].

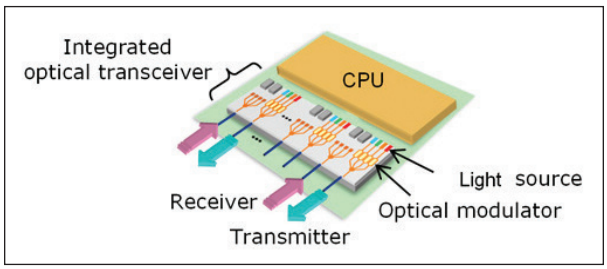

Figure 2: 2.5D integration of optical and electrical IC (CPU) [2]

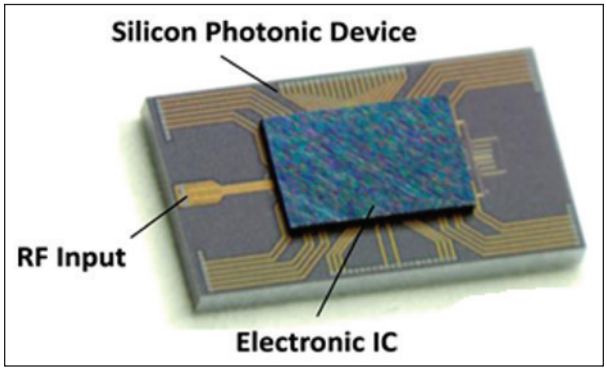

Figure 3: Packaging of an electronic IC (driver) on a silicon photonic device using a flip-chip bonding process - © IOP 2016 [3]

Fortunately, the ESD rating for these interfaces can be reduced. Because this flip-chip assembly is performed in an ESD controlled environment, the ESD protection level could be reduced to 200V HBM or sometimes even 100V HBM without effect on the yield. Because the high-speed interfaces are not exposed outside of the product/package assembly, they need to be considered as inter-domain interfaces.

Many advanced CMOS foundries provide a set of I/O and ESD protection circuits that designers can use. However, these standard, general-purpose, interface blocks are not suitable for the Silicon Photonic designs for the following reasons:

- The leakage from the general-purpose ESD blocks is too high
- The high-speed interfaces typically operate at a voltage level below the standard I/O voltage levels (1.0V or lower compared to 1.8V, 2.5V or 3.3V for the IO circuits)
- The high-speed SerDes circuits cannot tolerate a lot of parasitic capacitance or resistance added to the signal path. A typical analog I/O introduces 150fF of parasitic capacitance, well above what can be tolerated by the circuit.

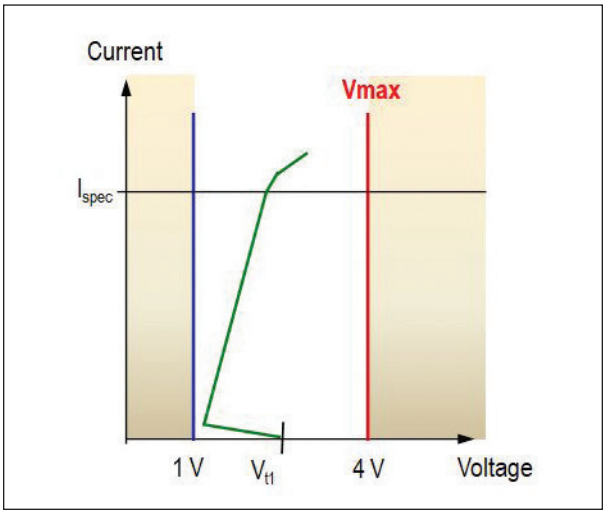

Figure 4: ESD design window for the 28Gbps interface in 28nm CMOS. The ESD protection trigger voltage must be below 4V, and failure current must be above 130mA (200V HBM)

Companies developing optical communication products are looking for improved solutions for the protection of the high-speed interfaces (Tx, Rx), and the low voltage power pads on the electronic die. Two case studies are included below.

EXAMPLE 1: ESD PROTECTION FOR 28GBPS INTERFACE IN 28NM CMOS

For the regular, low speed I/Os at 1.8V, the Analog/digital I/O library provided by the foundry was sufficient. The ESD requirement for those pads was 2kV HBM. On the other hand, the analog I/Os in the foundry library introduced too much parasitic capacitance for the high-speed interfaces. The designers requested a reduced total capacitance of the ESD device below 15fF.

The 28nm CMOS SoC was co-packaged with a silicon photonic device in a shared/hybrid integrated package. The assembly is performed in an ESD controlled environment. The ESD protection level was reduced to 200V HBM [9], roughly 130mA during 100ns TLP stress.

The 28Gbps interfaces used a differential pair concept. The 1V functional circuit is created using 0.9V core transistors to ensure the switching speed can be reached. However, these transistors are very sensitive during ESD stress. The available ESD design window (Figure 4) for the Rx, Tx signals is reduced to 4V. Other requirements for the ESD protection included low leakage operation and small silicon footprint (right side of Figure 5). The leakage at 1V bias is below 50pA at room temperature and less than 50nA at 125°C.

The ESD protection design consists of a full local protection clamp concept (Figure 5 on page 15). A 1V power clamp was integrated to ensure all the stress cases could be handled locally at the interface, and bus resistance is taken out of the equation. The entire clamp structure was isolated from the substrate to reduce noise from the substrate that could come from digital circuits further on the die.

The total parasitic capacitance at the I/O pad consists of different aspects. The junction capacitance can be easily derived from the foundry provided Spice models for diodes. The metal connections to the local ESD clamps can add a significant amount of capacitance. The parasitic metal capacitance can be derived from PEX (parasitic extraction) calculations. Reducing the width of the metal connections can reduce the capacitance but will also

reduce the robustness of the connection. The minimal metal width is derived from ESD stress performed at different metal stripes on our ESD test chip. Metal dummies (a requirement for CMP in advanced processes) are included in the PEX extraction when customers request ESD protection with ultra-low capacitance (well below 100fF).

Through an iterative process (layout, PEX extraction), the total parasitic capacitance of the ESD clamp was reduced to less than 15fF. The plot shown in Figure 6 illustrates the capacitance value as a function of the bias voltage at the pad.

In the iterative process to reduce the contribution of the parasitic capacitance from the metal connections, a number of rules are used:

- Remove unnecessary via connections
- Reduce Metal 1 as much as possible, keep it on top of the connected diffusion only.
- Prevent running Metal 1 across junctions.
- Vertical connection to higher-level metal layers to reduce capacitance from intermediate metal levels

Even when reduced, more than 40% of parasitic ESD capacitance can be linked to the metal connections in advanced nodes.

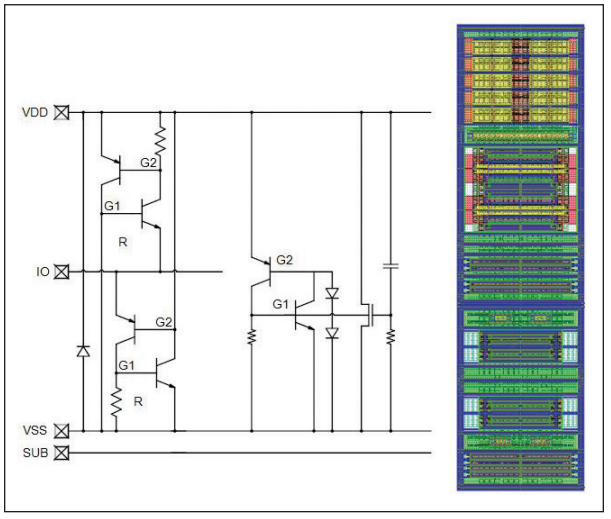

Figure 5: Schematic view (left) of the full local protection approach for the Rx and Tx nodes of the SerDes circuit. It is based on Sofics proprietary ESD-on-SCR devices. An SCR based 1V power clamp is integrated into the same layout (right). The total area for ESD is 683.75 um².

EXAMPLE 2: SILICON PHOTONICS SOLUTION ON N7 FINFET

To further increase the bandwidth of the optical interconnects (beyond 56 Gbps), our customer moved to TSMC 7nm FinFET technology. The proposed ESD solution is similar to the previous case (Figure 5). Two versions of the ESD protection are created, one with parasitic capacitance of 50fF, and a smaller version with less than 15fF. Measurements on TSMCs 7nm FinFET process demonstrate that the SCR based local clamp performs as expected (Figure 7).

In 7nm technology, the failure voltage of core transistors (gate to source and drain to source) is about 3V.

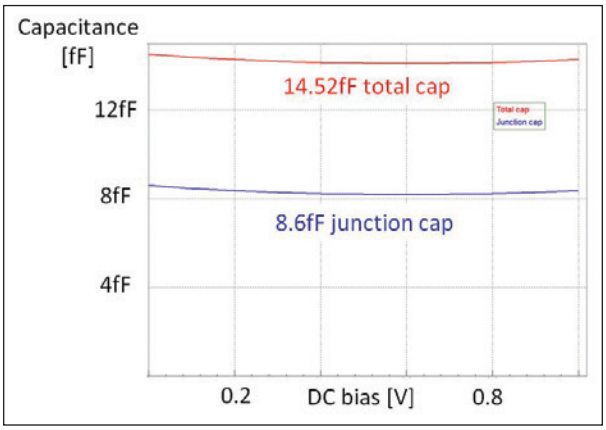

Figure 6: Parasitic capacitance (total and junction only) across the I/O voltage for the full local ESD protection clamp designed in a TSMC 28nm technology

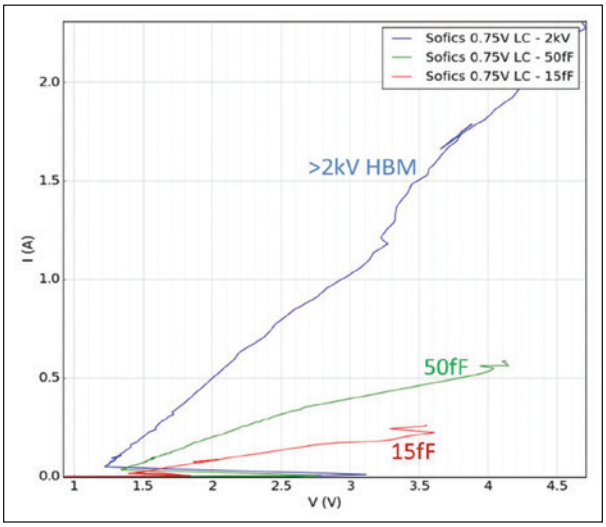

Figure 7: Silicon results on the TSMC N7 process. TLP results for three versions (with different target requirements) of the ESD concept.

Fortunately, in many SerDes applications, there is a bit more margin due to other transistors connected in series. Failure voltage under ESD conditions of those circuits is around 4-5V depending on the circuit concept – similar to the design window shown in Figure 4.

The 7nm low-capacitance ESD clamps have been integrated into two designs for high-speed interfaces. The simulated parasitic capacitance over IO voltage for the 15fF version is shown below (Figure 8) for the Typical, Fast and Slow corners. It includes both the junction capacitance (from the Spice model) and Metallization capacitance (based on PEX extraction). The SerDes circuits typically operate below 1V.

Besides low parasitic capacitance, the SCR based solution also has a low leakage, orders of magnitude lower compared to the ESD solution proposed by the foundry. The leakage measurement for the 15fF version is shown in Figure 9.

CONCLUSION

Silicon photonics can enable a strong growth of the (optical) communication market. Thanks to the mass production opportunity of both the optical and electrical dies and the availability of 2.5D and 3D hybrid integration all the requirements can be met: lower power, lower cost, high volume, high bandwidth.

High-speed SerDes interfaces integrated with Silicon photonics products need adequate protection with minimal parasitic capacitance. In this article, we demonstrated ESD protection clamps for 28 to 56Gbps interfaces in TSMC 28nm and TSMC N7 FinFET. Record-low parasitic capacitance levels below 20fF were achieved while ESD robustness is guaranteed.

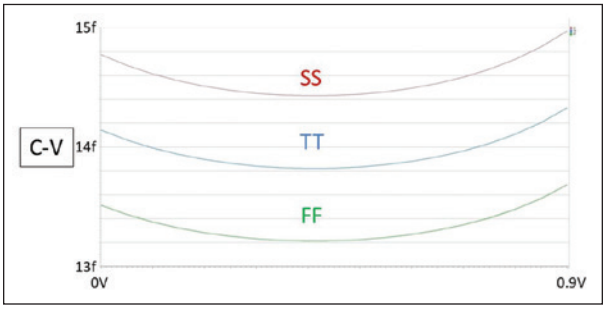

Figure 8: Simulation of the parasitic capacitance of the 15fF version on 7nm, across applied IO voltage, and for three corners.

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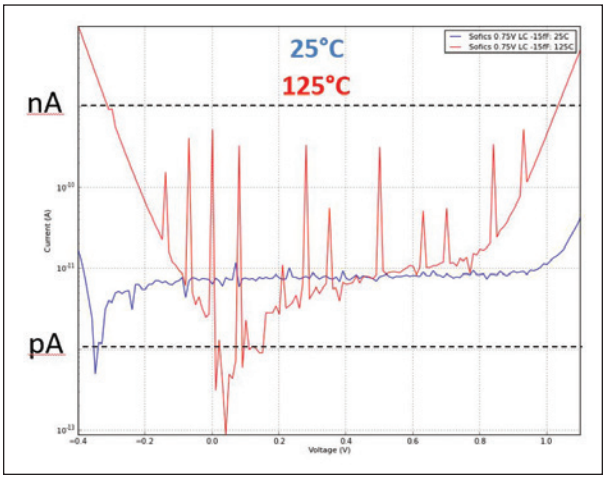
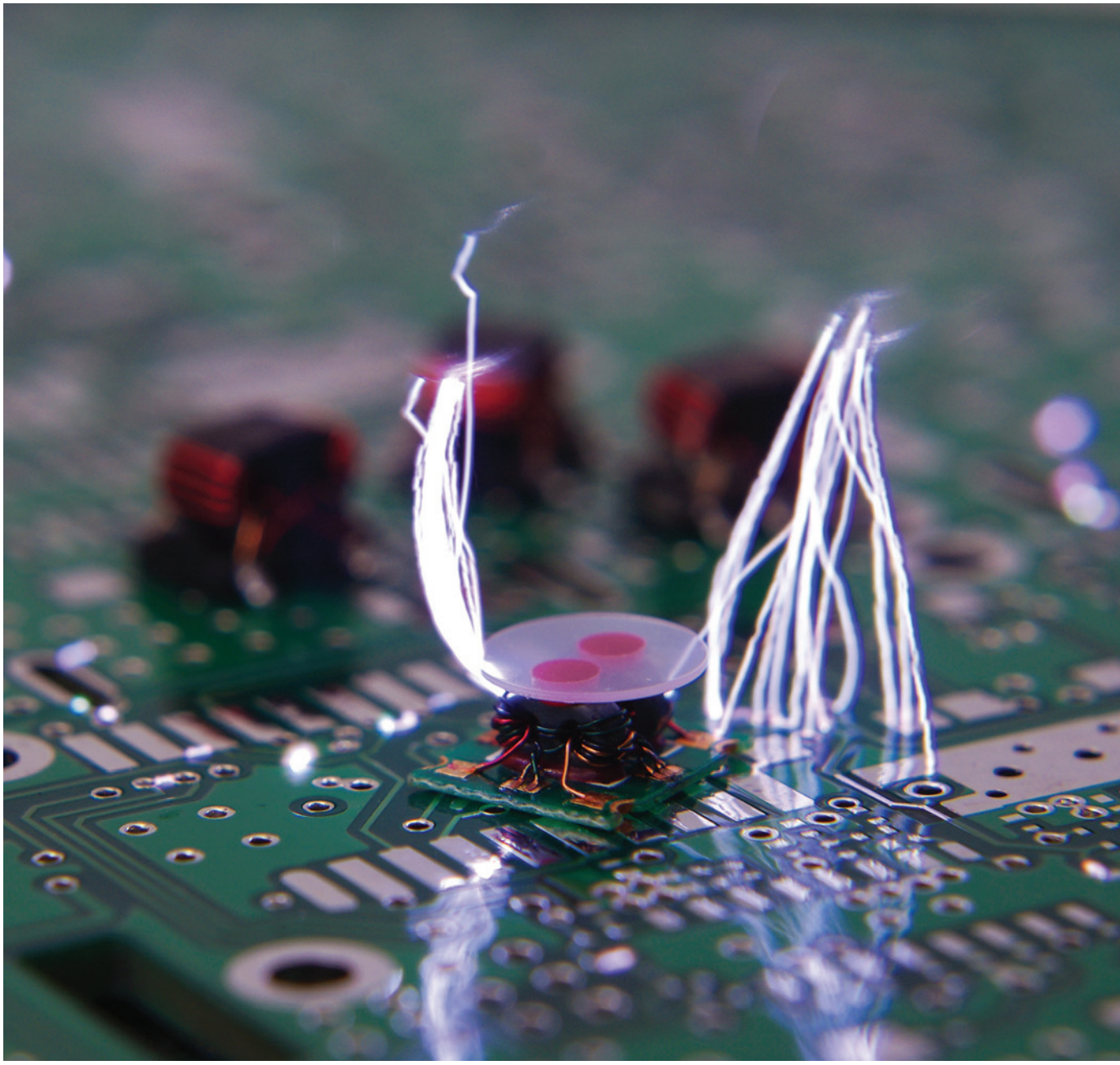


Figure 9: Leakage measurement at low (25°C) temperature and high (125°C) temperature. Even at high temperatures, the leakage of the ESD solution remains below 1 nA within the entire voltage range (0 to 0.75V).

DEVICE FAILURE FROM THE INITIAL CURRENT STEP OF A CDM DISCHARGE



By David Johnsson, Krzysztof Domanski and Harald Gossner

Editor's Note: *The paper on which this article is based was originally presented at the 40th Annual EOS/ESD Symposium, where it was awarded the Symposium Outstanding Paper in 2019. It is reprinted here with the gracious permission of the EOS/ESD Association, Inc.*

INTRODUCTION

RF interfaces tend to get more sensitive as the gate oxide (GOX) thickness is continuously decreasing for every new technology node. At the same time, the high operating frequencies limit the capacitive budget for Electro Static Discharge (ESD) protection devices. This makes the ESD design challenging, especially for the Charged Device Model (CDM) pulse with its high current and fast rise time. In this work the CDM failures of a sensitive RF interface are investigated. By modifying a CDM tester it is proven that the failures are related to the fast current step that appears at the beginning of a CDM event. The analysis is supported by 3D electrical field simulation of a CDM tester, showing that the first current step can have a rise time in the order of 20 ps. It is shown that the failure can be reproduced by applying CC-TLP pulses with 20 ps rise time. By investigations of rise-time sensitive test structures on wafer, it is demonstrated how the wiring layout can strongly influence the failure level in this fast pulse regime.

INVESTIGATED DEVICE

The device in this study is a Low Noise Amplifier (LNA) manufactured in a 28-nm technology. The input stage consists of thin-GOX MOS transistors with a breakdown voltage around 5 V. Due to RF performance requirements, the gate is tied directly to the pad, which is critical from an ESD point of view. The chosen ESD protection scheme is a standard rail-based topology as shown in Figure 1. To meet the capacitance requirement of <180 fF, small diodes were used as ESD clamping devices. The diodes have no Shallow Trench Isolation (STI) between the anode and cathode diffusions, and thus exhibit a fast turn-on time [1]. All protection devices, including a large dedicated power clamp, were placed in a close vicinity to the LNA (max 100 µm) to avoid any inductive paths and to minimize the bus resistance. The LNA is located directly below the input ball of the package. Since the receiving gates of the LNA are connected directly to the pad, a GOX damage can be detected by DC leakage testing.

TEST RESULTS

VF-TLP Results

In an early design phase the LNA circuit was placed on a test chip, using a very similar topology as expected for the final LNA implementation. Testing was performed on wafer level using a VF-TLP test system with 1ns pulse width and 100 ps rise time. The result from VF-TLP testing is shown in Figure 2 on page 20. The achieved robustness in the range of 5-6 A was considered sufficient to handle the minimum CDM requirement of 250 V. Identical values were obtained with 300 ps pulse rise time. TLP testing on the final packaged product showed identical results.

CDM Results

The packaged LNA interface was tested on an Orion 2 CDM tester with a JS-002 compliant test head.

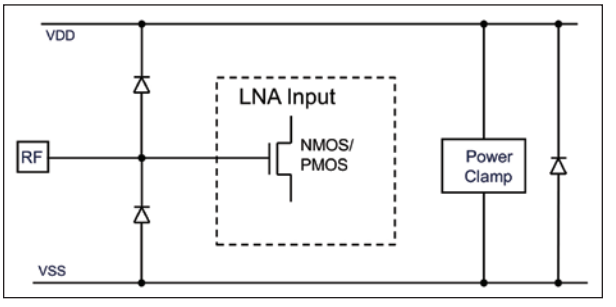


Figure 1: ESD Protection circuit for the LNA interface.

The results are presented in Table 1. Unexpectedly, the LNA failed at +250 V at a peak current of 2.7 A. This is only about half the current compared to the VF-TLP test results at negative polarity (corresponds to positive CDM stress). For the negative CDM stress polarity, the device failed at -400 V.

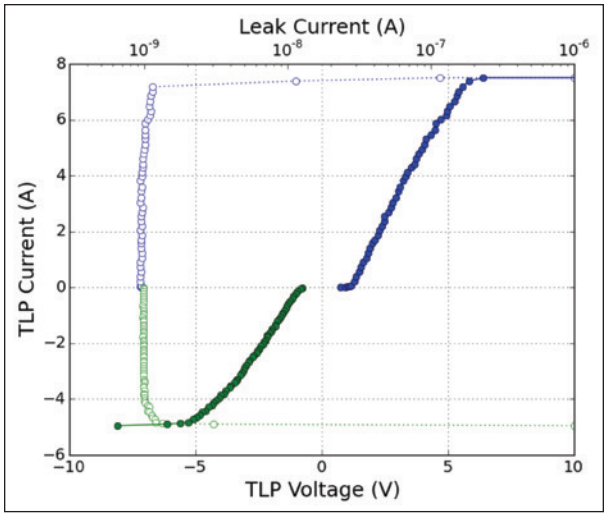


Figure 2: VF-TLP Results from an LNA test structure on wafer. The pulse width is 1 ns and the rise time is 100 ps.

Level	Peak Current	Pass/Fail
+200 V	2.4 A	Pass
+250 V	2.7 A	Fail
-350 V	-3.6 A	Pass
-400 V	-4.2 A	Fail

Table 1: CDM results for LNA interface.

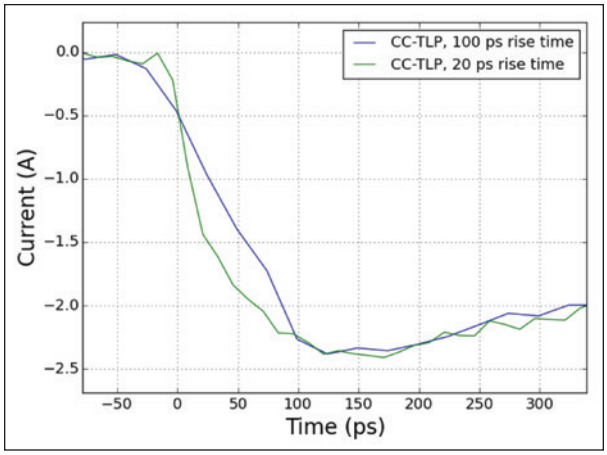


Figure 3: Measured pulse rise times of CC-TLP pulses at -2.4 A stress level (33 GHz measurement bandwidth)

CC—TLP Results

The packaged LNA was tested with a CC-TLP setup [2] with a pulse source capable of rise times as low as 20 ps. Captured pulses into the device with 100 ps and 20 ps rise time are presented in Figure 3, and the CC- TLP test results in Table 2. At 100 ps rise time the currents resulting in failure are very similar to the VF- TLP results. However, at 20-ps rise time failures appear at a peak current as low as -2.4 A. Hence, it is evident that the failure is not caused by the peak current, but rather by the rise time of the pulse. This is consistent with [3], where it was shown how the current slew rate influences the fail level of a device in

CC-TLP Rise Time	Positive Fail	Negative Fail
100 ps	>+6 A	-7 A
20 ps	+3 A	-2.4 A

Table 2: Results from CC-TLP testing

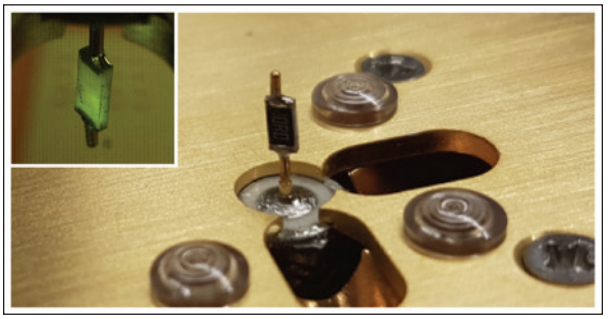


Figure 4: CDM discharge head with a size 0603 chip resistor soldered in series with the pogo pin

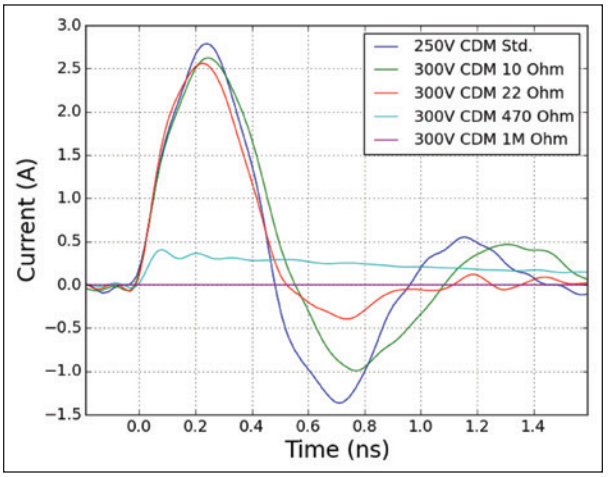


Figure 5: CDM discharge waveforms with different resistors inserted in the pogo pin

a CC-TLP setup. Note that in the case of 20 ps rise time the measured current through the device shows a fast rise time only up to 70% of the peak current, followed by a slower rise up to 100%. Tests performed on a short circuit (metal plane) showed identical waveforms, so the limited rise time seems to originate from a limited bandwidth of the CC-TLP probe.

CDM TESTER ANALYSIS

Series Resistance in the Pogo Pin

In this experiment, the pogo pin was cut, and a chip resistor of size 0604 was soldered in series, as shown in Figure 4. The resulting discharge currents are shown in Figure 5, and the results from LNA product testing in Table 3. As expected, the peak current decreases with increasing resistance. The most interesting results were obtained with the 1 M-Ω resistor: Although the captured current was practically zero, fails at +250 V were still observed. The failure mechanism seems to depend only on the CDM charge voltage, not on the measured current. It should be pointed out that most CDM current probes have a limited bandwidth of only a few GHz [4]. Possibly, an important part of the waveform is not captured.

CDB Current into the Popo Pin

In simple LRC models, the pogo pin inductance defines the rise time of the CDM pulse. However, the simple model does not take into account the stray capacitance

CDM Setup	Level Peak	Current	Pass/Fail
Standard Pogo	+250 V	2.7 A	Fail
22 Ω	+300 V	2.4 A	Fail
470 Ω	+300 V	0.4 A	Fail
1 MΩ	+200 V	~0 A	Pass
1 MΩ	+250 V	~0 A	Fail

Table 3: Results from CDM tests with resistor in the pogo pin

of the pogo pin. In the presented experiments with the 1-MΩ resistor in the pogo pin, the 2-mm-long tip has a certain capacitance to the surrounding (ground plane, charge plate, and to the device), as represented in Figure 6. Hence, a dipole charge is present at the pogo pin. When a device is discharged by the pogo pin, a current flows into the pogo-pin tip and charges its capacitance. Even though the pogo-pin capacitance is comparably small, the current can be considerable since there is only a small inductance in the path.

CDM Head S-Parameter Simulation

In [5] a method was demonstrated for measuring the S-parameters of a CDM head and simulating the resulting waveforms. In this work, we apply the same methodology but simulate the S-parameters with the 3D field solver HFSS from Ansys. Figure 7 shows the models used for simulation of the CDM head with and without resistor. The S-parameters are simulated at the excitation port between the pogo pin tip and the charge plate. The 1-MΩ resistor is simplified as a block of alumina interrupting the pogo pin.

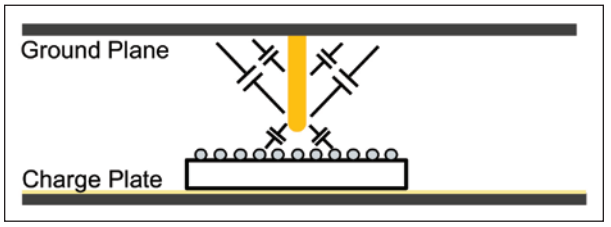


Figure 6: Capacitance contributions of the pogo pin

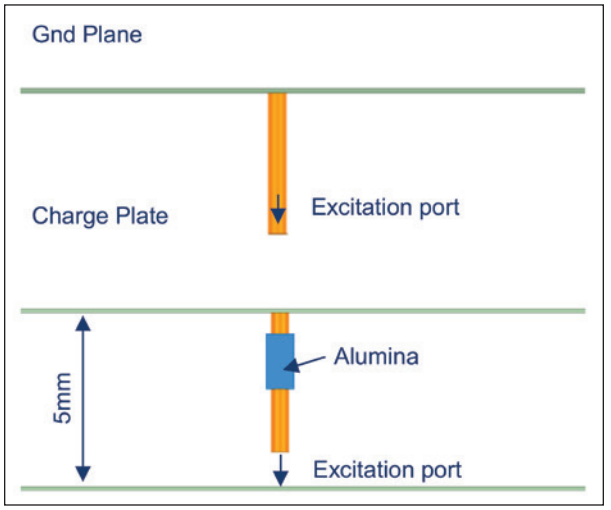


Figure 7: Side view of the 3D models used for simulation of a CDM head with standard pogo pin (top) and resistor in the pogo pin (bottom).

Figure 8 shows the simulated Z-parameters for the two configurations. Z-parameters are derived from the S- parameters and are easier to read since they represent the impedance seen into the pin tip. In the low frequency range the impedance decreases with increasing frequency as expected from a capacitance. For the standard CDM head the inductance of the pogo pin starts to dominate above 500 MHz and the impedance increases with the frequency. However, above 10 GHz the inductance loses its effect and the impedance remains in the order of 100 Ω up to 100 GHz. In this frequency range, the impedance with and without the resistor is similar. Thus, it is mainly the frequency spectrum of the discharge spark that determines the pulse shape in the upper frequency range, and it will be similar for the standard and the 1- MΩ pogo pin.

Rise Time of the CDM Spark

The most uncertain property of a CDM discharge event is the spark rise time and resistance. It varies strongly, depending on the applied voltage, air

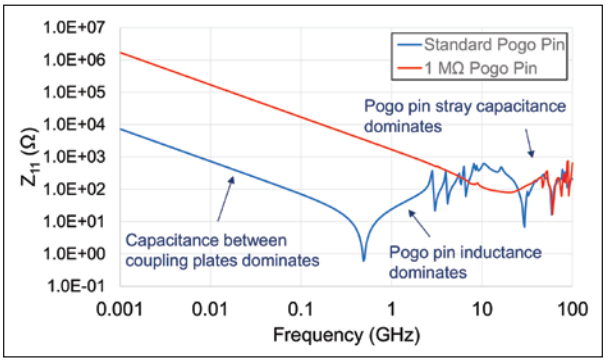


Figure 8: Simulated Z-parameters for a standard CDM head (blue), and a CDM head with 1-MΩ resistor in the pogo pin (red)

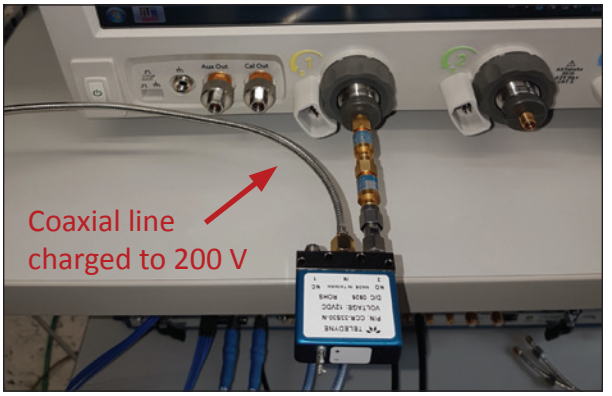


Figure 9: Measurement setup to characterize the pulse rise time from a coaxial switch

humidity, ball and pogo pin geometry and the speed of approach. In [6] it was shown that a CDM-like discharge between metal parts can have a rise time around 30 ps. To characterize an ideal metal-to-metal discharge a standard coaxial switch with 26 GHz bandwidth was used. The switch was connected in a TLP-like configuration with one port connected to a coaxial line that is charged up to 200 V. The other port of the switch was connected via attenuators directly to the input of an oscilloscope with 33 GHz bandwidth, shown in Figure 9. The coaxial switch is not an ideal TLP switch and shows strong pulse instability. Still, it was possible to capture several pulses with a rise time as low as 20 ps, as shown in Figure 10. Since

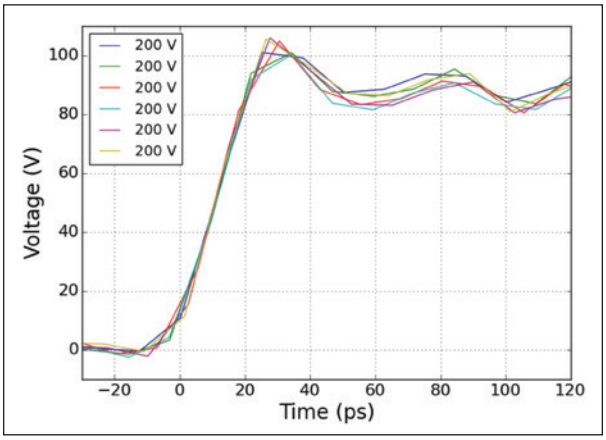


Figure 10: Discharge waveforms from a coaxial switch at 200V charge voltage

the overall bandwidth of the setup is limited by the 18-GHz rated connectors and attenuators, the rise time might be even faster. In this publication, a spark rise time of 20 ps was chosen for the simulations.

CDM Current Simulation Results

Simulation of the CDM current was performed in ADS from Keysight. The simulation schematic is presented in Figure 11. Since the simulated CDM head S-parameters don't contain any package capacitance or spark resistance, the components C package and R spark have been added. C package was chosen to 3 pF to fit the CDM pulse shape, and R spark to 25 Ohm. The simulation results are presented in Figure 12 on page 24. The blue curve shows the discharge current from a standard CDM tester. Note that there is a first step in the waveform with about the 20-ps rise time of the pulse source. This corresponds to a current wave propagating along the pogo pin towards the ground plane, just like in a transmission line. When the wave reaches the ground

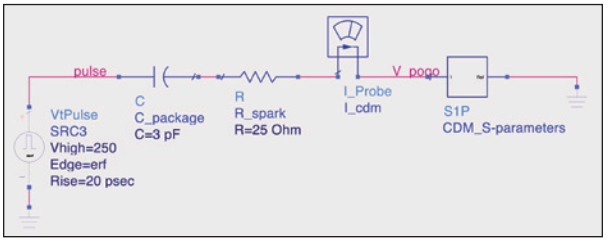


Figure 11: Schematic for CDM current simulation with S-parameters in ADS

plane, it gets reflected with a negative factor due to the low impedance of the ground plane. As a result, the amplitude is about doubled when the reflected wave reaches the pogo pin tip after about 50 ps. The current keeps increasing in steps until the peak amplitude is reached.

The first step also exists with the 1-MΩ resistor in the pogo pin, but the amplitude returns to zero after

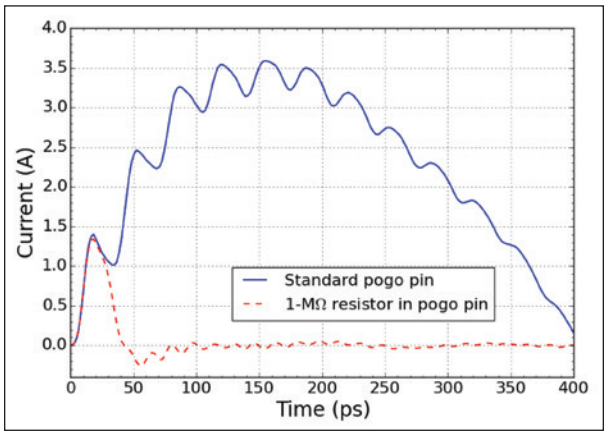


Figure 12: Simulated current entering the pogo pin with a standard pogo pin (blue) and a 1-MΩ resistor in the pogo pin (red)

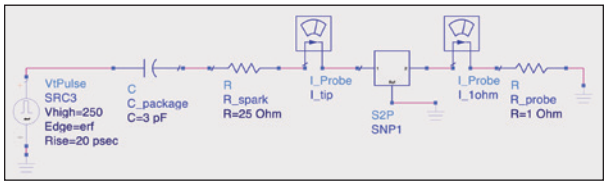


Figure 13: Schematic to simulate the current measured by an ideal 1-Ω CDM probe

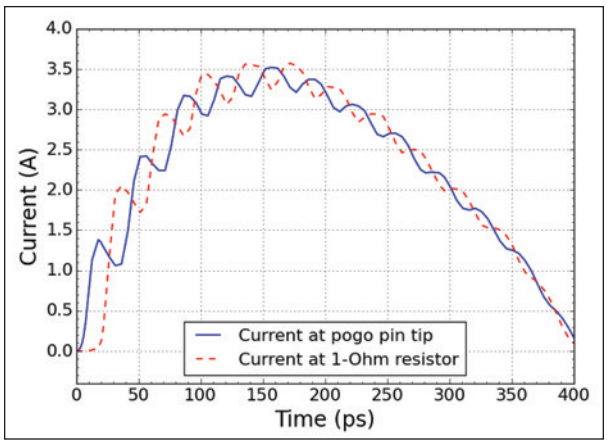


Figure 14: Simulated current of the current into the pogo pin tip (blue) and through the 1-Ω resistor of a CDM probe (red)

40 ps since the resistor blocks the current flow. The comparison of both discharge waveforms and the fact that the damage occurs at the same CDM voltage level clearly demonstrates that the LNA is damaged by the current step at the onset of the CDM discharge.

According to the simulation, the first step has an amplitude of about 1.4 A at 250 V charge level. This appears to be in the same range as where the LNA failed in CC-TLP testing with 20 ps rise time, considering that the CC-TLP probe was only capable of delivering a fast rise time up to 1.5 A according to Figure 3.

With such fast current slew rates, wire inductance and ESD device turn-on time play an increasing role. Even short traces with an inductance in the order of

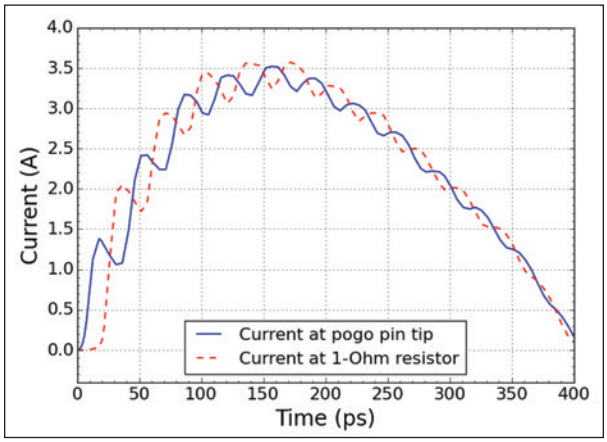


Figure 14: Simulated current of the current into the pogo pin tip (blue) and through the 1-Ω resistor of a CDM probe (red)

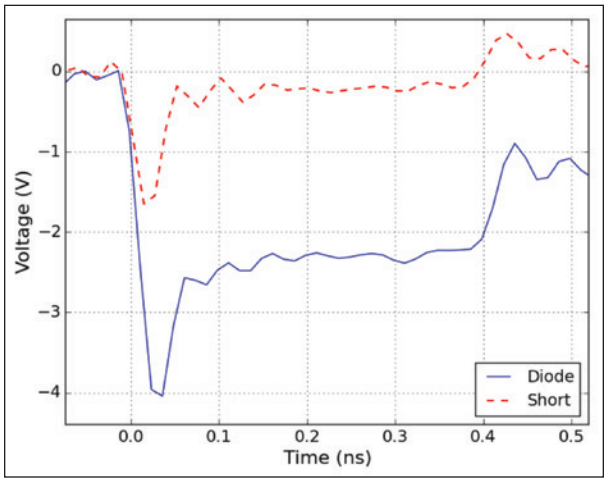


Figure 15: Voltage response of the ESD diode (blue), and the de-embedding structure (red) at -3 A TLP with 20 ps rise time

10 pH will create a voltage drop of several volts. For RF optimized designs with a short low-loss path from the ball to the sensitive gate, this poses a serious threat that needs to be addressed in the ESD design.

Can a CDM Tester Measure the Fast Rise Time?

CDM probe heads with a bandwidth of 20 GHz have been reported [7], but can a CDM probe head really measure the current at the pogo pin tip? This is investigated by performing a simulation with an additional excitation port between the pogo pin and the ground plane. The CDM waveform is simulated with an ideal 1-ohm resistor to ground at the second port according to Figure 13. Hence, the current flowing through the 1-ohm resistor to the ground plane can be obtained, which is the current an ideal CDM probe would capture. The simulation result is presented in Figure 14. It is seen that an equally fast rising pulse arrives at the 1-Ω resistor with a time delay of about 20 ps. However, the current of the first step has a higher amplitude than the current entering the tip. This can be explained by the impedance mismatch that appears when terminating the pogo pin into a 1- ohm load. Theoretically, the current would double when terminating into close to a short circuit, but since the pogo pin is not a perfect transmission line, there will be losses.

It has been shown that a CDM probe head can principally measure the fast initial step, but the waveform will not be identical to the current entering the pogo pin.

TLP TESTS WITH 20-PS RISE TIME

Diode Performance

To assess the performance of the ESD protection a diode test structure on wafer was measured with the fast TLP source presented in section IV.B.2. The diode size was about twice as large as used in the ESD protection for the LNA. RF probes of type Cascade Infinity with a bandwidth of 40 GHz were used in TDT configuration. With a fast rise time of 20 ps the wiring inductance will cause a considerable inductive voltage drop. In order to eliminate this contribution, a de-embedding structure with the same metallization, but short-circuited in the lowest metal layer, was also measured. Hence, it is possible to assess the voltage contribution from the diode alone by subtracting the de-embedding waveform. In Figure 15 the voltage response of both the diode and the de-embedding structure at a current of -3 A are plotted. The voltage response after subtraction of the de-embedding waveform is presented in Figure 16 on page 26.

The diode shows 2 V clamping voltage with an overshoot of 0.5 V. This should be considered a very fast diode with a turn on time of less than 50 ps. This can typically not be achieved with STI-bound diodes or SCR based devices.

LNA Test Structure TLP Results

To assess if these diodes can protect the LNA sufficiently, two different structures on wafer level were tested, as shown in Figure 17 on page 26. Both structures use an LNA monitor device consisting of the transistors of a typical LNA. Test structure LNA1 has the VSS and VDD connections of the LNA monitor connected directly at the VSS/VDD nodes

of the ESD diodes. LNA2 has the VSS of the LNA connected to the VSS rail with a 40-µm long trace. These test structures are only suitable for negative TLP testing, since the power clamp (not shown in the figure) is insufficiently connected with relatively large inductance. The results from TLP testing with 20-ps rise time are presented in Figure 18. LNA1 (with the short VSS connection) fails at -6 A current, which is about the same value as obtained from VF-TLP testing of the packaged LNA product with a rise time of 100 ps. This means that the fast rise time of 20 ps can be handled by the circuit. The small overshoot of the diodes is not harming the LNA gate oxide. LNA2, on the other hand, shows a much lower failure current of -3 A.

Analysis of the Failure of LNA2

The lower failure level of -3 A for LNA2 can be explained by the additional voltage drop appearing across the vertical connection down to the VSS rail. In Figure 19 the current path from the VSS pad to the RF pad has been drawn for LNA2. It is evident that the voltage drop across the vertical VSS trace between the diode and the VSS rail will be visible at the LNA monitor. It can be estimated that the 40-µm long trace will have about 40 pH of inductance. The resistance in the path is in the order of milliohms and can be neglected.

With a current slew rate of 3 A in 20 ps the voltage drop can be expressed as:

V = dI/dt * L = 3 A / 20 ps * 40 pH = 6 V

It seems plausible that an additional voltage drop of 6 V is enough to damage the gate oxide of the LNA monitor even for the very short stress time of 20 ps.

A similar VSS routing weakness could be identified in the LNA product. After redesign with improved routing, the product was able to meet the CDM requirements.

CONCLUSION AND OUTLOOK

It has been shown that the fast initial step of the CDM pulse damages the sensitive GOX of the investigated LNA. The exact rise time is not accessible, but it could be proven to be 20 ps or less. All test methodologies using 100 ps rise time failed to reproduce the CDM failure by a factor of two. This applies to VF-TLP and CC-TLP, but would also be the case for alternative CDM testing methods such as Contact CDM (C-CDM) or CDM2.

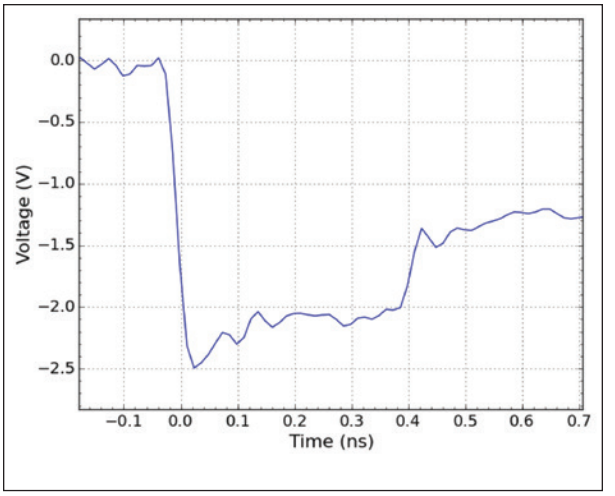


Figure 16: Voltage response of the ESD protection diode, de-embedded by subtracting the wiring contribution

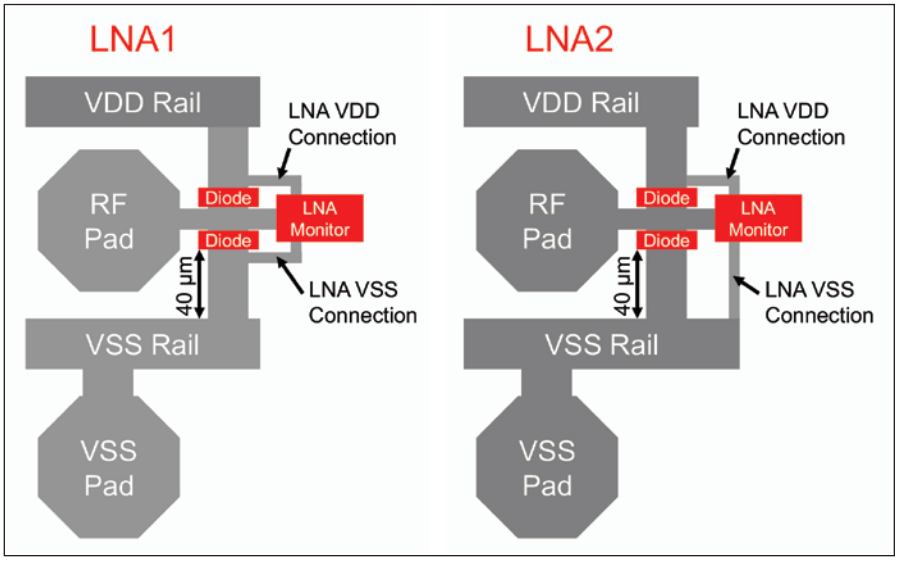


Figure 17: LNA test structures LNA1 with short VSS connection (left) and LNA2 with long VSS connection (right)

The failure mode from CDM testing could be reproduced by applying CC-TLP stress with a rise time of 20 ps. However, it is not straight forward to correlate the CC-TLP current slew rate with a certain CDM stress level. For the investigated LNA the CC- TLP fail level for positive and negative polarity only differed by 25% (+3 A / -2.4 A). However, in CDM testing the difference was as high as 60% (+250 V / -400V). This discrepancy is not yet understood, but it is believed that the polarity might have an impact on the spark rise time. These phenomena need to be fully understood before alternative CDM stress methods can be applied for qualification.

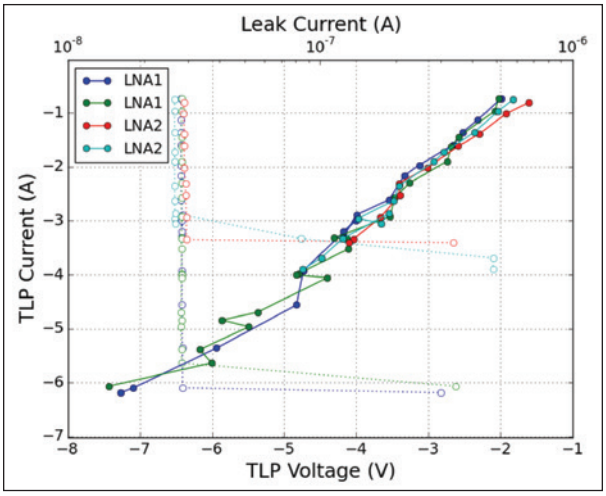


Figure 18: VF-TLP result for the LNA test structures measured with 20 ps rise time

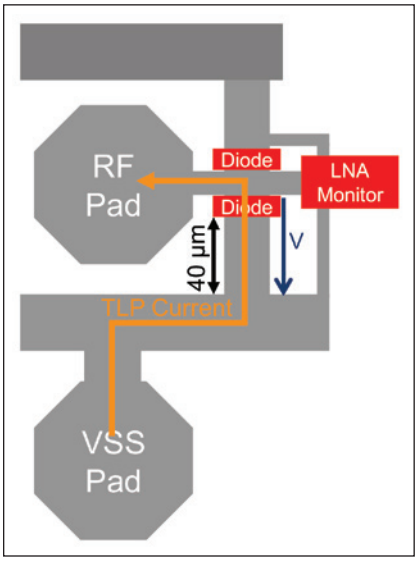


Figure 19: TLP current flow in test structure LNA2 for a negative pulse on the RF pad

Since the exact voltage level in a CDM tester varies in a wide range depending on the calibration, the level of the first step will depend on the calibration as well. This introduces an additional source of error.

As perspective to real-world relevance, it should be mentioned that the first current step should not be considered as a tester artifact. The phenomenon takes place whenever a charged device is approached and touched by any metal object.

An improved high bandwidth TLP characterization method is needed to accurately assess the ESD design of sensitive RF interfaces.

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EOS/ESD Symposium Preview

42nd Annual EOS/ESD Symposium – A Brand New Hybrid Event Experience!

The EOS/ESD Symposium represents the world's leading forum on electrostatic discharge and electrical overstress. This year, we are thrilled to invite you to experience our brand new hybrid event. With our hybrid event, you can attend the Symposium face-to-face and we are following the most advanced safety precautions available. You may also experience the Symposium in real-time via livestream or enjoy On-Demand access after the live event concludes from the comfort of your home or office. The choice is yours!

Since 1979, industry professionals from all over the world have flocked to the EOS/ESD Symposium to enjoy the unique opportunity to meet professionals with hands-on experience in their fields as well as learn from and exchange knowledge with the greatest industry experts of our time. This is an exciting time, and we are committed to bringing you a one-of-a-kind hybrid event that sets the bar high, pioneering a new vision for our events, and setting a path for others to follow.

We are proud to offer you 3 tracks over 5 days of tutorials and technical presentations. These will feature different delivery mechanisms and will involve ways for you to engage presenters virtually if they or you are present at the face-to-face event! Instructors and presenters will be live at the event, some will be presenting from their home base via livestream broadcasting to the event site, and some will provide a pre-recorded presentation and join us for Q&A sessions. We also welcome you to enjoy industry exhibits from exhibitors showcasing a wide variety of ESD solutions from established products to leading-edge innovations, on-site and also through virtual exhibits.

On top of these incredible offerings, we are also pleased to present this year's Keynote "The Role of Photons in Hardware Security" by Dr. Shahin Tajik of the Florida Institute for Cybersecurity (FICS) Research at the University of Florida who is joining us via livestream.

When it comes to registering for the 2020 EOS/ESD Symposium, you have options. You can choose to register for face-to-face Symposium attendance, register to enjoy the event in real-time livestream, or register for Symposium On-Demand access after the event to enjoy on your own time! Face-to-face and livestream registration also include 30 day access to On-Demand as a bonus. All of these options feature our exhibitors face-to-face and virtually.

To learn more about Symposium, view the program, and see all of the registration options that we have to offer, please visit https://www.esda.org/events/42nd-annual-eosesd-symposium-and-exhibits.

KEYNOTE

Tuesday, September 15
9:00 am - 9:45 am

The Role of Photons in Hardware Security

Dr. Shahin Tajik, Florida Institute for Cybersecurity (FICS) Research at the University of Florida

Live-Stream

42nd Annual EOS/ESD Symposium – A Brand New Hybrid Event Experience!

A hybrid event is a combination of presentations delivered in person, by livestream or and on-demand recording.

Presenters can be present at the event giving their presentation, off-site streamed live or recorded for on-demand offerings.

Attendees can be present at the event or view all the symposium offerings from the comfort of their home/office either live or on-demand.

Symposium On Site

If you are attending the Symposium in Nevada, here is what you can expect:

- Speaker can be onsite giving presentation
- Speaker can be giving presentation by video (live)
- Pre-recorded video of presentation(s)
- 30 days access to on-demand Symposium (excludes tutorials)
- Complimentary access to onsite exhibits and virtual exhibits

Tutorials On Site

If you are attending the Symposium in Nevada and sign up for a Tutorial(s) here is what you can expect:

- Instructor can be onsite giving tutorial
- Instructor can be giving tutorial by video (live)
- Complimentary access to onsite exhibits

Tutorial Livestreaming

If you want to view livestreams of tutorials, here is what you can expect:

- Livestream link for selected tutorial
- Instructor will be onsite giving tutorial
- Instructor will be giving tutorial by video (live)

Symposium Livestreaming

If you want to view livestreams of the Symposium content, here is what you can expect:

- 1 link (3 total) for each parallel track (Zoom links)
- Speaker can be onsite giving presentation
- Speaker can be giving presentation by video (live)
- Complimentary access to virtual exhibits
- 30 days access to on-demand Symposium (excludes tutorials)

On-Demand Offerings

If you want to experience the Symposium On-Demand, here is what you can expect:

- Tutorials are pre-recorded videos (view at your convenience)
- Symposium presentations are recorded live (either speaker was on-site giving presentation or live from off-site)
- Pre-recorded video of presentation(s)
- 30 days access to selected offering(s)
- Complimentary access to virtual exhibits

ESD ASSOCIATION®

WHY YOU SHOULD PAY ATTENTION TO CABLE DISCHARGE EVENTS (CDE)

CDE, the Re-Discovered Barrier in the ESD Landscape?

Cable discharge events (CDE) occur when a cable is plugged into an electrical system and when the cable and the system are at different potentials. CDE can cause system failures such as system lock up, requiring a reboot, and even physical damage.

There have been numerous technical papers on the subject, and ESDA Working Group 14, System Level ESD, has been considering the development of a test standard to screen for this issue for some time. The problem is that there is no single "worst-case" event that is CDE. There are many types and qualities of cable, multiple ways that cables and system can get to different potentials before being connected, and the far end of the cable may or may not be connected to another electrical system or device.

In this article we will review our current understanding of some of the issues with CDE. At the same time, we welcome your help in developing a CDE test method (or methods) to address the issues you have encountered. Please contact us to share your own experiences with CDE, and the real-world problems you believe we need to consider in this process.

INTRODUCTION

A signal interface cable is considered as a point-to-point connection between two ports. The side where the cable-to-port connection is to be made is called the near-end port. The far-end port may be left open or connected to some other system/device, which itself might also be connected to something else.

Mart Coenen has been an independent industry consultant for more than 25 years following his career with Philips Electronics. He has been involved with international standardization development since 1988, and formerly served as the chair of the IEC 61000-4-2 technical committee (TC/SC 77B). Coenen currently serves on a number of ESDA standardization committee working groups, and can be reached at mart.coenen@emcmcc.nl.

By Mart Coenen

For the signal interface, there are three cable options, shielded, non-shielded and double shielded. The shielded cable options include cables for microphones, coaxial, USB-2/-3 or (S)STP connections. Non-shielded cable options include cables for loudspeakers, earphones, UTP, USB-1, USB-x for charging, etc. Double shielded cable options include cables such as HDMI and Firewire (see Figure 1), where the inner high-speed signal wires are screened by an inner shield and separated from and outer shield that is typically connected to the metal outer shell of the connector.

We'll discuss three interface use-cases, as follows: 1) unconnected charged cables (Use Case #1); 2) charged cables which are at their far-end already connected to some other circuitry, without protective earth (PE) connection (Use Case #2a); or 3) charged cables connected to some other circuitry with a PE connection (Use Case #2b).

Use Case #1

In the unconnected charged cable case, typically, the outer cable screen (for shielded cable) or the (unshielded) wires will be charged up: Q = C.V. After a while, all inner wires will obtain the same potential against their (conductive) surroundings (for example, the outer shield). The total charge becomes distributed, that is, there is almost no potential difference among the inner wires or between the inner wires against the outer screen.

However, how the discharge event will occur is determined by the first contacted terminal at the connector versus socket and/or screen of the cable. Due to the contacting, the charge distribution in the cable as well as on the outside of the cable towards the surroundings will change rapidly but with different impedance paths and different time constants.

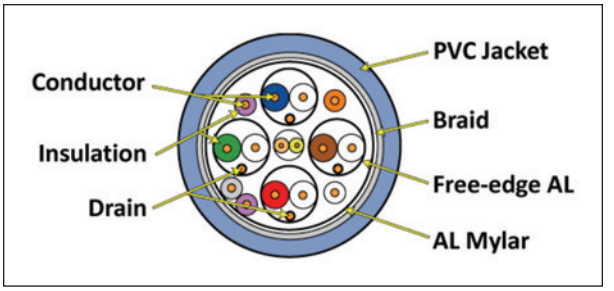

Figure 1: HDMI cable cross-section showing inner and outer shields. With HDMI, (FireWire) the inner and outer shields remain separated between shell and pins.

Due to the mini- and micro-pitch spacing between connector terminal contacts, the maximum static voltage that may occur between the separate wires and/or the wires and the outer screen will be limited to less than 1 kV. However, an unconnected cable can be charged up to several kV's. Short lasting pulses may have higher voltages without causing instant breakdown.

Cable charge build-up may arise from dielectric friction, rubbing, airflow and many man-made kinds of disturbances. Potential changes also arise from lifting up the charged cable, thereby lowering the capacitance → increased voltage: V = Q/C.

Use Case #2

In the case where the far-end of the cable is (already) connected to some circuitry (for example, a mouse, keyboard, display, beamer, storage device, tablet, laptop, PC, charger, supply, server, switch, router, test and measurement equipment, etc.), the charge storage will be determined by whether that far-end system/device is connected to PE. The internal electronic circuitry connected to the signal interface wires is either floating (Use Case #2a) or intentionally kept insulated (Use Case #2b, see Figure 2 on page 32)

from the conductive enclosure, which is electrically coupled to that PE terminal.

For battery or interface wire supplied devices (Use Case #2a), the far-end termination will be capacitively coupled to its surroundings. In this case, the (conductive) exterior of the far-end device is not connected to PE. When the far-end system/device is locally supplied, while the inner electronics are kept insulated (e.g., Class-II electric devices; without PE, or Class-I electric devices with PE), a "Faraday cup" is created. The maximum potential is limited by the creepage and clearance distances used or by the break-down voltage of the capacitors used, crossing that insulation barrier. This far-end floating circuitry is connected to the inner wire of the cable. Any retention voltage may be stored in-between that floating circuitry (that is, inner wires) against the outer shield (i.e., AC mains and/or PE). Making "shell contact first" will affect the CDE, such that the maximum discharge current will result due to the low(er) impedance path which closes the loop.

If the device at the far-end is affected by an EMC transient threat (e.g., EFT, Surge), it will couple immediately onto the cable interface in either Use Case #2a or #2b. With the regulatory EMC tests, coupling is done to the cable's exterior at the near-end port while the cable is fixed to the equipment under test (EUT), not while the cable is in the process of making its contact. True, the probability of the coincidence of an EMC related threat while plugging in a cable is low, but this combination will be very harsh.

(It is important to note that EMC immunity tests are intended to show recoverable functional behavior of a system rather than physical damage at the component level!)

THE CAUSE FOR OVERSTRESS IS IN THE DETAIL

When a "floating" charged signal cable is plugged into a port, the internal discharge event will initially look like a regular transmission line pulse (TLP), starting at t = 0 ns, of which the pulse duration is determined by twice the propagation delay of that cable for all far-end load conditions (see Figure 3). The typical duration of a TLP test pulse according to applicable ESDA, JEDEC and IEC standards is 100 ns. The maximum cable length is determined by the interface (for example, 5 meters for USB-2, 15 meters for HDMI, etc.).

Considering the propagation speed in cables of ~ 7 ns/m, 15 meters HDMI cable would yield a pulse length of 210 ns. The exterior propagation speed on a cable will be equal to the speed of light, that is 3.3 ns/m. The rise time of the pulse while making contact will be in the sub-nanosecond region, considering a metal-to-metal contact. The maximum voltage to be expected on the cable may be high for the cable as a whole (up to several kVs) but will be internally limited considering screen-to-wire or wire-to-wire, typically less than 1 kV.

The discharge "source" impedance, voltage-over-current ratio, will be determined by the cable cross-sectional topology and whether the impedance is determined in the cable itself (that is, wire-to-wire(s) or wire(s)-to-screen) or from the whole cable towards its surroundings. The exterior cable to surroundings'

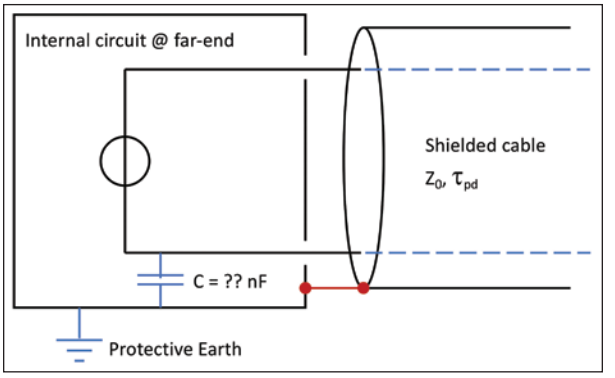

Figure 2: Unknown far-end capacitance (Use Case #2b) between floating circuitry and PE

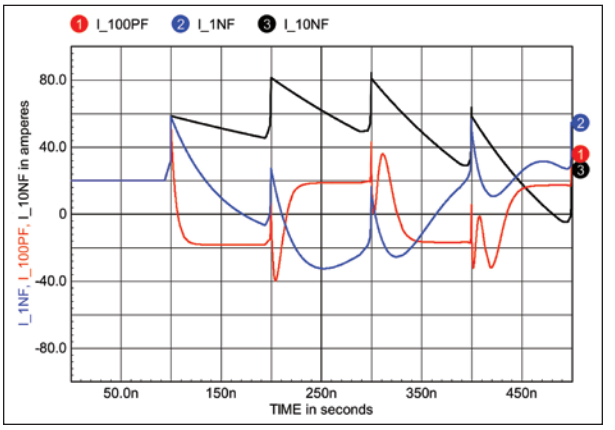

Figure 3: Discharge current (voltage across 1 Ω) of a 50 Ω TLP (100 ns) charged up to 1 kV (initially 20 Amps) while far-end loaded by 100 pF; lower red curve, 1 nF; blue curve and 10 nF; black curve).

impedance is 100 to 300 Ω. The inner wire-to-wire or wire to screen impedance is 50 to 100 Ω. At worse, the characteristic impedance of the inner-to-outer shield transmission line (HDMI, FireWire, etc., see Figure 1) can be below 10 Ω.

From a formal TLP source, the peak current can be directly calculated from the initial charge voltage on the line and the characteristic impedance. For a 1 kV charged up 50 Ω transmission-line, the peak current will be 20 Amps initially. A TLP source with an additional capacitance at the far-end means that the initial current will again resemble the TLP characteristics. After twice the propagation delay of the cable is used, the charge as stored in the far-end circuitry will show up too.

As an example, the 100 pF case results when a USB cable with a mobile phone attached at one end is plugged into a computer (to perform a backup, for example). In case the phone is already electrically connected to a sound system (headphone) while the USB cable is plugged in, values of 1 nF or higher occur. Issues like these can be circumvented by using wireless BT interfaces instead. This might also answer the question of why new mobile phones no longer include a headphone socket and use contactless charging. If there are no accessible ports, the likelihood of CDE vanishes too.

This article may prompt other questions. But, after the initial hang-up or damage to a port, it's unlikely that you have conducted your own experiments to learn what went wrong and why. In many cases, when the product is still under warranty, the product will be sent back to the supplier for repair. But repairing the damage alone contributes nothing to our understanding of the application condition that caused it.

CONCLUSIONS

CDEs are likely to occur anytime a cable is plugged into a port (in particular, when the cable is loaded capacitively at the far-end), though they often go unrecognized.

An unconnected cable may collect charge such that its potential towards its surroundings becomes over 1 kV and will increase when being lifted up. In-between the wires and/or the wires and a screen, CDE will remain less than 1 kV due to the mini- and micro-pitch of the connector pins.

However, if the far-end of a cable is loaded by some insulated circuitry, the total capacitance for charge storage will increase towards the outer shield. The maximum potential will be limited as described above. The total charge energy ($E = \frac{1}{2}C.V^2$) will be substantially higher than with "formal," non-far-end loaded TLP test cases.

Do you have an increase in unexplained ESD/EOS failures on your connector ports? Do you think that you have suffered a CDE leading to soft- or hard-failures that have not shown-up with regular ESD compliance testing? Or have you passed IEC system and other ESD qualifications but fail miserably when working with certain cables from a new supplier or other connected far-end devices? If so, you may suffer from CDE, a re-discovered interaction between cables and systems that can cause profit loss, WIP repair and retention, and unsightly internet product reviews.

We want to hear your CDE stories and your experiences in working to minimize CDE risk. So feel free to write to us at iwannarockcde@emcmcc.nl.

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WHY RESISTANCE REQUIREMENTS DIFFER BY INDUSTRY AND WHY STANDARDS MATTER

An access floor contractor was bidding a project calling for "static dissipative" flooring. Like many contractors, the project manager viewed the terminology from a generic perspective. Most laymen equate the term static dissipative (SD) with any flooring type that is marketed for the purposes of mitigating the discharge of static electricity. They do not realize there is a distinction between a conductive floor and a dissipative floor and that there may be a practical reason for choosing one over the other.

Since the architectural specs did not include electrical resistance parameters, cite-specific industry standards, or require that resistive properties be tested before final acceptance, the project manager felt comfortable bidding any type of ESD flooring. In this instance, she proposed a conductive floor for an FAA flight tower, when in fact the FAA requires flooring to measure in the static-dissipative range.

Similar scenarios occur every day. The root causes almost always involve semantics, with specifiers citing incorrect standards for a specific industry, as well as a general lack of understanding about electricity and static-control flooring.

This creates multiple problems encompassing product liability, economic loss, failure to perform and in compliance with industry standards.

Dave Long is the CEO and founder of Staticworx, Inc., a leading provider of flooring solutions for static-free environments. He has 30-plus years of industry experience and combines his comprehensive technical knowledge of electrostatics and concrete substrate testing with a practical understanding of how materials perform in real-world environments. Dave can be reached at dave@staticworx.com.

By David Long

CONFUSING CONDUCTIVITY AND SPECIFICATIONS

To investigate this dilemma, we need to explore the history of floors used to prevent static-discharge problems.

The roots of the ESD flooring industry hark back to the need for preventing static sparks in medical environments where flammable and explosive gases were administered as anesthesia. Like the static-control wrist straps used in electronics manufacturing today, early versions of static-control products involved some form of single-point grounding and bonding (via tethering) to maintain a single potential between all conductors that came in contact with one another. In general, this was achieved by placing wet towels across the floor to connect the anesthesiologist's foot with the base of a steel operating table. (Yes, this is real!)

In an article published in 1926, titled "How Can We Eliminate Static from Operating Rooms," Dr. E. McKesson writes:

> *"Hence the simplest method of preventing static sparks is to keep the objects concerned in the administration of combustible mixtures in contact—i.e., the patient, the anesthetist and the inhaler. This is usually done and accounts for the relative infrequency of fires from static sparks in the operating room."*[1]

As throughout the electronics industry today, McKesson recognized that full reliance on a multi-step human process of tethering and un-tethering of personnel and fixtures with cords and wires assumes a perfectly executed process every time. He writes, "But errors of technique are made, and if the conditions are 'right,' a fire occurs."

McKesson recognized the need for a passive grounding system that does not rely solely on a series of connections that may not always occur. McKesson writes:

> *"An effort has been made at one hospital to make errors impossible by grounding a mosaic floor, consisting of alternate block of tile and bronze in one or two rooms and a solid metal floor in another. That is, when one steps upon this floor the charge on his body flows through a thick wire to the ground. The operating table, apparatus, instruments, anesthetists, surgeons and all are thus grounded or their charges neutralised."*

McKesson wrote this paper for the British Journal of Anaesthesia – advocating for what we now call ESD flooring - all the way back in 1926. And yet, into the 1960s, there continue to be records of hospitals placing wet towels on the floor to provide electrical bonding between the anesthesiologist and the operating table.

Late in 1950, a Wisconsin company called Natural Products began work on plastic conductive flooring. The following year they would introduce Statmate and rename the company Vinyl Plastics Inc (VPI). VPI's non-metallic conductive floors gained immediate and widespread acceptance as a highly effective grounded flooring solution in hospitals. Unlike metal, these early conductive plastic floors could be made with inherent and controlled electrical resistive properties. This was and is critical to electrical safety.

Circa 1950, the NFPA had determined that floors in hospitals should not measure below 25,000 (2.5×10^4) ohms or in excess of 1,000,000 ohms (1.0×10^6). Vinyl floors could be manufactured to meet this requirement. This ohms range of 2.5×10^4 to $< 1.0 \times 10^6$ marks the launching point at which today's confusion about conductivity, resistance ranges, and the suitability of conductive floors begins.

RESISTANCE TESTS PER NFPA GUIDELINES ARE NOT EQUIVALENT TO ESD/STM 7.1 TESTS

Although metal floors were durable and provided effective conductivity, they offered absolutely no

safety in the presence of alternating current (A/C). To ensure safety along with a reliable level of conductivity, NFPA bulletin 56 (issued in the 1940s) required a specific electrical resistance range for conductive floors. Electrical resistance was to be tested using an ohmmeter, with 500 volts of applied current. This was because, in 1950, meters – 500 volts was chosen to test for resistance with an emphasis on electrical safety. Wall-mounted meters, such as the Conductometer were installed in ORs and tested both flooring and footwear at 500 volts. Today we test with 10 volts of applied current.

Why does this matter? Ohm's Law: the higher the applied voltage, the lower the resistance. Likewise, the lower the applied voltage, the higher the resistance.

Since ANSI STM 7.1 requires 10-volt electrification, resistance tests of the same material will measure much higher than an NFPA test using 500 V of applied current. Likewise, the results of an NFPA test using 500 V of applied current will be much lower than the results of a test following guidelines of 7.1 applying 10 V. The point is that the test methods are not equivalent; therefore, measurements are not equivalent.

The Electrostatic Discharge Association (ESDA) and the electronics community have chosen an upper limit of less than 1,000,000 ohms for defining a conductive floor.[2] This conductive range is quite different from the range set by the NFPA. Yet many floorings suppliers state that their floors measure above 25k ohms per NFPA - but also market their floors as measuring between 25k and one million ohms per the current ANSI/ESD STM 7.1 10-volt test method.

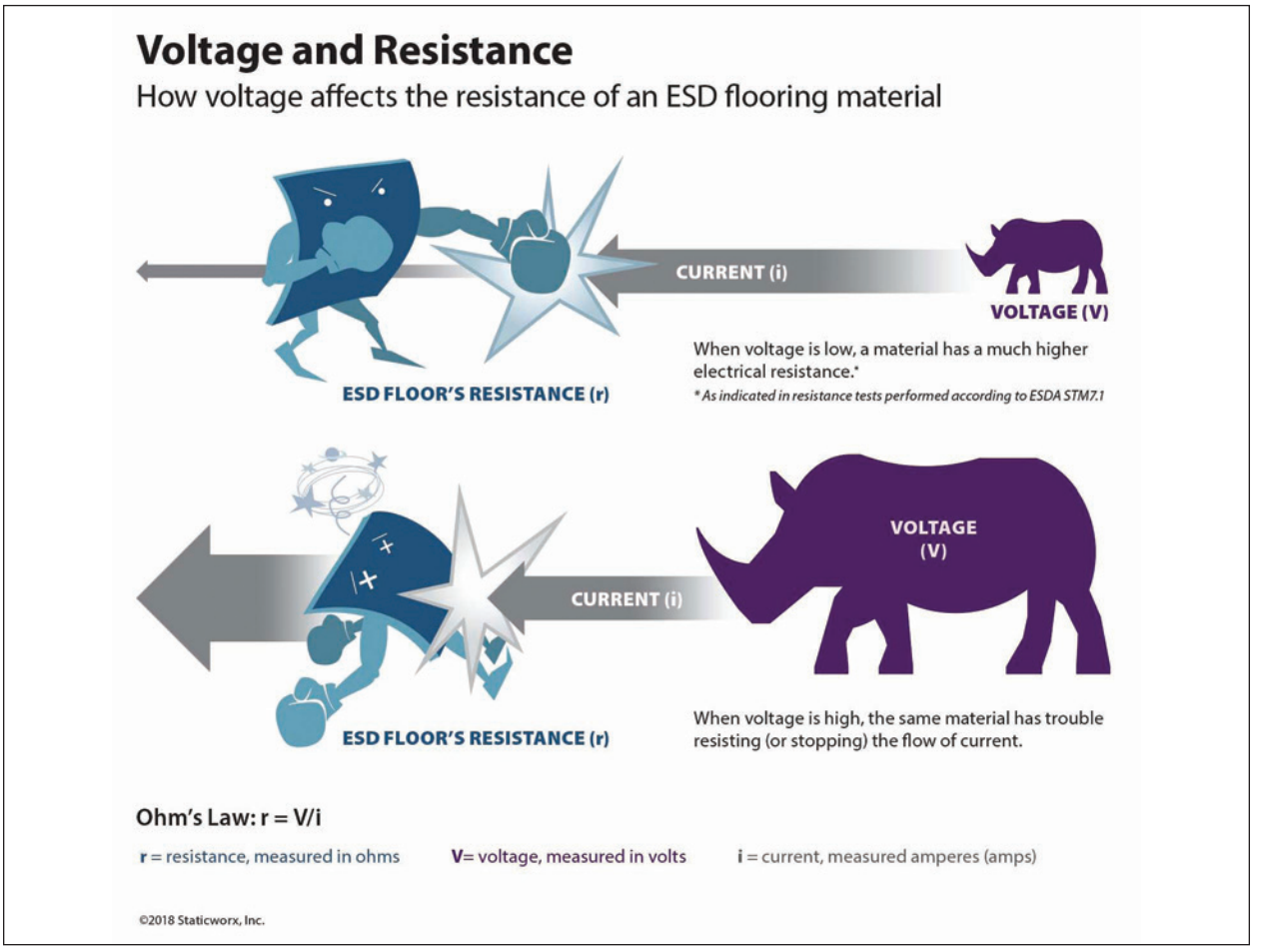


Figure 1: How voltage affects the resistance of an ESD flooring material

This is not possible. A floor measuring 25,000 ohms at 500 volts will present as a much less conductive surface with 10-volt electrification. The chart in Table 1 shows measurements taken by an independent lab. As indicated in the chart, gray ESD carpet measuring 75,000 ohms with 10 volts of applied current measured only 16,000 ohms at 500 volts. While the floor tested per S7.1 measured slightly above the stated 25,000 ohms, when tested at 500 volts, it failed to meet the NFPA's requirement for resistance.

Table 1 shows examples of the discrepancy between resistance test results performed per NFPA and ANSI/ESD test methods.

WHAT IS A STATIC-DISSIPATIVE OR CONDUCTIVE FLOOR?

This history of conductive flooring and evolving resistance test methods brings us to the concerns we face today. What is a static-dissipative floor, what is a conductive floor, and which version should be referenced in a specification?

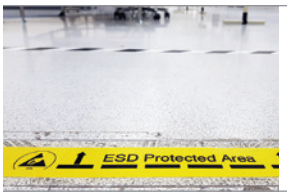
The first answer is actually a question. What are the test methods you're using to measure resistance and what standards do you need to meet for compliance in your industry? One example is NFPA 99. Almost every flooring manufacturer mentions NFPA 99 compliance; NFPA 99 deleted any mention of floor testing years ago due to the elimination of flammable anesthesia. Unless the manufacturer specifications account for and incorporate test data obtained at 500 volts, they are misapplying a defunct test method.

The perhaps bigger problem is that different industries have different resistance standards. We often see ANSI/ESD S20.20 cited in specifications for ESD floors for 9-1-1 dispatch centers. ANSI/ESD 20.20 relates specifically to electronics manufacturing and handling environments and requires the use of ESD footwear in the qualification of ESD flooring. ESD footwear is never used in call centers and dispatch areas. In these applications, the mention of 20.20 is irrelevant and potentially misleading. Floors in these environments should reference either Motorola R56 or ATIS 0600321, both of which require floors to measure between 1.0×10^6 and 1.0×10^{10}. Many airport flight towers are also equipped with static-control floors. Like Motorola R56 and ATIS 0600321, FAA-STD-019f, Lightning and Surge Protection, Grounding, Bonding, and Shielding Requirements for Facilities and Electronic Equipment, prohibits the use of flooring measuring below 1.0×10^6 due to concerns for the safety of people working near energized equipment.[3]

Unlike end-user spaces, there is no lower resistance limit for flooring used in an ANSI/ESD S20.20 ESD program. Conductive floors are an important element in an ANSI/ESD 20.20 program due to the need for worker mobility, rapid charge decay, prevention of tribocharging, effective grounding of mobile workstations and the ability of personnel to handle

Carpet Tile Test Results for product marketed as measuring 2.5×10^4 – 1.0×10^8:		
Color	***ANSI/ESD STM 7.1 @10 volts***	***NFPA @500 volts***
Grey	7.5×10^4	1.6×10^4
	7.2×10^4	1.4×10^4
Silver	7.5×10^4	1.4×10^4
	6.9×10^4	1.3×10^4
Dark grey pattern	5.0×10^4	1.4×10^4
	6.0×10^4	1.0×10^4
Carpet Tile Test Results for product marketed as measuring 1.0×10^6 – 1.0×10^9:		
Color	***10 volts***	***500 volts***
Patterned carpet	1.8×10^6	1.1×10^6
Blue Carpet	1.5×10^6	8.0×10^5

Table 1: Carpet tile resistance test results showing the discrepancy between NFPA and ANSI/ESD test methods



It is imperative that the end-user understands that the burden of liability involving both safety compliance and product suitability of electrically grounded flooring rests on both the manufacturer's and specifier's shoulders.

highly sensitive products without the use of wrist straps. ANSI/ESD S20.20 states that the resistance measurements obtained through the use of ANSI test methods are not to be used to determine the relative safety of personnel exposed to high AC or DC voltages. Although most flooring manufacturers do not produce flooring measuring below 25,000 ohms it is imperative that the end-user understands that the burden of liability involving both safety compliance and product suitability of electrically grounded flooring rests on both the manufacturer's and specifier's shoulders.

It should not be implied that conductive flooring is unsafe when appropriately utilized in an ANSI/ESD S20.20 certified program. These programs require regular testing of both floor conductivity and footwear conductivity, these spaces are accessed only by trained personnel and conductive flooring should never be installed in areas where high potential testing or equipment is in operation. However, before any conductive floor is installed, buyers should understand that a conductive or static dissipative floor is a system that requires multiple installation materials, special footwear and specific steps during the qualification and verification processes. As further confirmation that flooring should not be viewed as a discreet component, we need to look no further than the newly proposed tile in the 2020 draft of test method ANSI/ESD STM 7.1., Flooring Systems – Resistive Characterization.

TEST METHODS VERSUS PERFORMANCE STANDARDS

Most ESD flooring specifications reference some type of resistance testing procedure, such as those found in ANSI/ESD STM7.1, ASTM F150, DOD 4145.26 or NFPA 99 (formerly NFPA pamphlet 56). Many buyers mistake these test methods as representing performance standards. Performance standards guide the specifier in determining what test results are acceptable. Test methods tell us how to determine if we have compliant products.

For example, FAA-STD-019f states that a floor must measure between 10^6 and 10^9 ohms. Motorola R56 states that the floor should measure between 10^6 and 10^{10} ohms when tested per ANSI/ESD S7.1. ATIS 0600321 cites the same resistance requirements as Motorola R56. Although not an actual standard, IBM's Physical Site Planning document states:

> *"For safety, the floor covering, and flooring system should provide a resistance of no less than 150 kilohms when measured between any two points on the floor space 1 m (3 ft.) apart. They require a test instrument similar to an AEMC-1000 megohmmeter for measuring floor conductivity."*[4]

Like the hand crank meggers and other instruments used to test insulation resistance, the AEMC-1000 does not offer a 10-volt output but it does allow testing up to 500 volts. Since IBM's upper recommended resistance is 10^{10} and no test voltage is mentioned, one might believe that this test was intended to ensure a minimum amount of insulation resistance. By contrast, the ESD industry requires simply that conductive floors measure below 1.0 x 10^6 at 10 volts.

Again, resistance measurements alone should not be used to determine the safety of a particular floor. There are multiple reasons for this that are beyond the scope of this article. However, as an experiment, we solicited a third-party lab to apply both AC and DC voltages to various ESD floors and measure the resulting current at the floor-ground connection. The results of this testing are shown in Table 2.

As the chart illustrates, some conductive floors appear to enable significantly more electrical current than others. The amount of current is not accurately predicted mathematically by using electrical resistance measured with an ohm meter. In part this is due to the construction of conductive floors, whether they are comprised of composite layers, if they are fully conductive on the surface or constructed of the same material throughout the thickness of the material.

However, the experiment clearly illustrates what we already know: a floor with an inherent resistance over 1,000,000 ohms is less likely than a very conductive floor to enable a dangerous leakage current. This fact drives recommendations for using dissipative flooring in data centers, flight towers, dispatch operations and areas where energized equipment is used. Whereas we need to control static generation and charge decay to an extremely low threshold in electronics manufacturing, we do not need the same level of performance in end-user spaces like data centers, etc. While the electronics in these end-user spaces can be damaged by electrostatic discharge, they're less sensitive than components in manufacturing and handling facilities.

According to an ASHRAE white paper, the data center industry views 500 volts as an upper threshold compared with the 100 volt upper limit for meeting ANSI/ESD S20.20 in electronics manufacturing.

THE SEMANTICS PROBLEM

The ESDA has produced a glossary of terms. Three newly proposed terms referencing flooring include flooring systems, conductive flooring systems and dissipative flooring systems. But terms like dissipative and conductive are frequently misunderstood and misapplied. In some cases, the misapplication leads to problems in the field. In many cases, specifiers don't know which electrical range is the correct one for their client's specific industry. In other cases, specifications are copied from previous static-control projects even though the application may be entirely different.

For example, per DOD 4145-26-M, DOD explosives-handling applications require conductive floors as defined by resistance testing at 500 volts. Per ANSI/ESD STM 7.1, the same floor tested at 10 volts might actually measure in the very low part of the static-dissipative range. As previously noted, resistance is predicated by the applied voltage.

"To avoid any confusion and future liability due to misunderstandings about conductivity and test method, we recommend that explosives handling specifications always be cowritten by the end-user and the specifier."

Let's look at the definition of a dissipative flooring system. A static-dissipative flooring system, measured with a full combination of components, including surface material, adhesive, grounding mechanism, substrate and any other material in the system, is considered static dissipative as long as the system has a resistance greater than or equal to 1.0×10^6 ohms and less than 1.0×10^9 ohms.

This sounds like a comprehensive definition with no room for misunderstanding. However, if an installer laminated the highly conductive bronze tiles (mentioned in McKesson's 1926 article) with a static-dissipative adhesive, it would appear in a typical ANSI/ESD STM 7.1 resistance to ground field test that the bronze floor was not conductive, but, in fact, static dissipative. How?

Carpet Tiles with Black Backing - 2.5×10^4 - 1.0×10^8	
AC Volts Volts ac	**AC Amperes mili Amps ac**
4	1
11.5	3
18	5
30.5	**10**
52.3	**20**
117	**50**
EC Rubber Tiles - 2.5×10^4 - 1.0×10^6	
AC Volts Volts ac	**AC Amperes mili Amps ac**
31	0.1
40	0.4
66	2
80	4
93	5
120	7.6
Static Dissipative Carpet Tiles - 10^6 - 10^9	
AC Volts Volts ac	**AC Amperes mili Amps ac**
5	**<0.1**
10	**<0.1**
25	**<0.1**
50	**<0.1**
100	**<0.1**
120	**<0.1**

Table 2: Results of testing applying AC and DC voltages to various floor types

Because we would be grounding bronze through a series resistor network. The dissipative adhesive, not the bronze surface, would be the groundable point, and the adhesive would represent a false indication of the resistance to ground if the dissipative ground were bypassed due to an inadvertent connection to ground. Relying upon a less conductive surface as the groundable point below a more conductive surface is an imprudent concept for multiple reasons.

This may seem like a ridiculous example, except for the fact that many concrete on-grade substrates retain a high concentration of water due to the local water table. Water saturates adhesives, lowering the conductivity of the system, and changes the path to ground. This scenario occurs so often that flooring installers test concrete per ASTM 2170 for moisture, in part, to determine how vapor content and emissions in the substrate might negatively affect the adhesive.

What if this floor system were installed in a space where energized systems were resting on the floor while operating at 480 volts, three-phase. Obviously, any electro-mechanical system resting on the floor would become the groundable contact point and bypass the series resistor (dissipative adhesive) below the bronze tiles.

Another misstatement is the claim that "Flooring meets or exceeds ANSI/ESD S20.20." The first error is the failure to recognize that flooring is only one component of a system within a program that must comply with all aspects of a standard, which typically includes many items unrelated to the flooring itself. For example, ESD flooring, whether conductive or dissipative, is often mistaken as having only to ground people and prevent charge generation on people wearing ESD footwear.

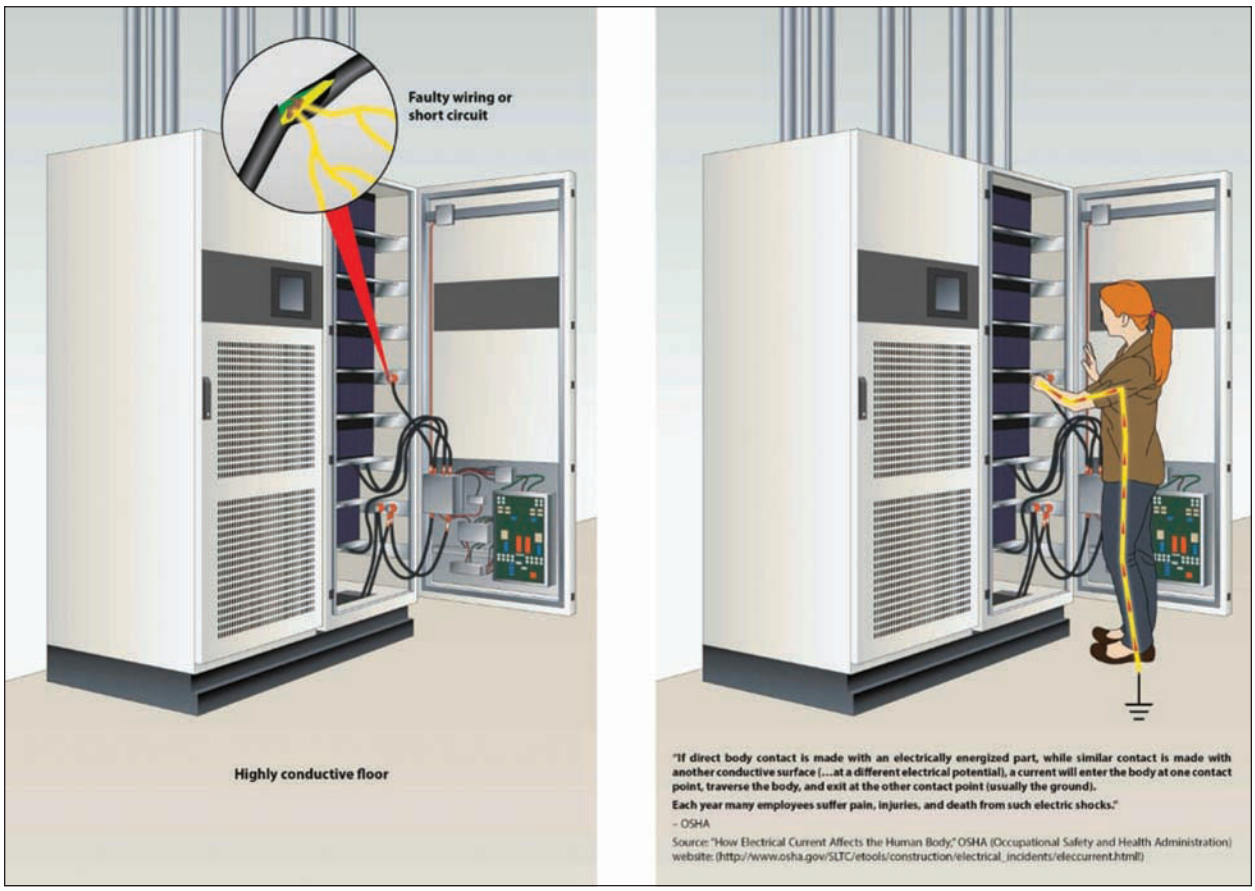


Figure 2: Large systems positioned on the surface of an ESD floor can inadvertently act as a surface ground connection.

This is not the case. Most users of ESD flooring rely on the floor to ground and prevent charges on people, carts, shelves, benches and chairs. Due to surface hardness or spacing of conductive surface particles, a particular design conductive floor may do an excellent job of grounding and charge prevention on personnel but fail at grounding mobile carts and shelving. If a circuit board manufacturer expects the floor to provide a path to ground for workstations and carts and the floor fails in this task, it cannot be described as meeting S20.20, whether or not the root cause of failure is the drag chain on the cart, the contact area of the conductive casters, or the arrangement of conductive layers or conductive particles embedded into the flooring.

If we remove the question of which standards are better or more valid or more clear, we are left with the most important question: Why would one write a specification for a specific industry and fail to mention the standard for that industry? Now we are back to the beginning: semantics, incorrect standards cited for a specific industry, and a general lack of understanding about electricity and static-control flooring.

What happens when an industry or entity like the FAA publishes a frequently updated 500-page grounding standard and specifiers, installers or facilities managers neglect to follow the standard? This question may be one for the product liability attorneys, but over the course of several discussions, liability attorneys tell me that meeting standards is a "minimum expectation." In the case of ESD flooring and electricity, this means privileging safety equal to or greater than potential performance enhancements from increased conductivity.

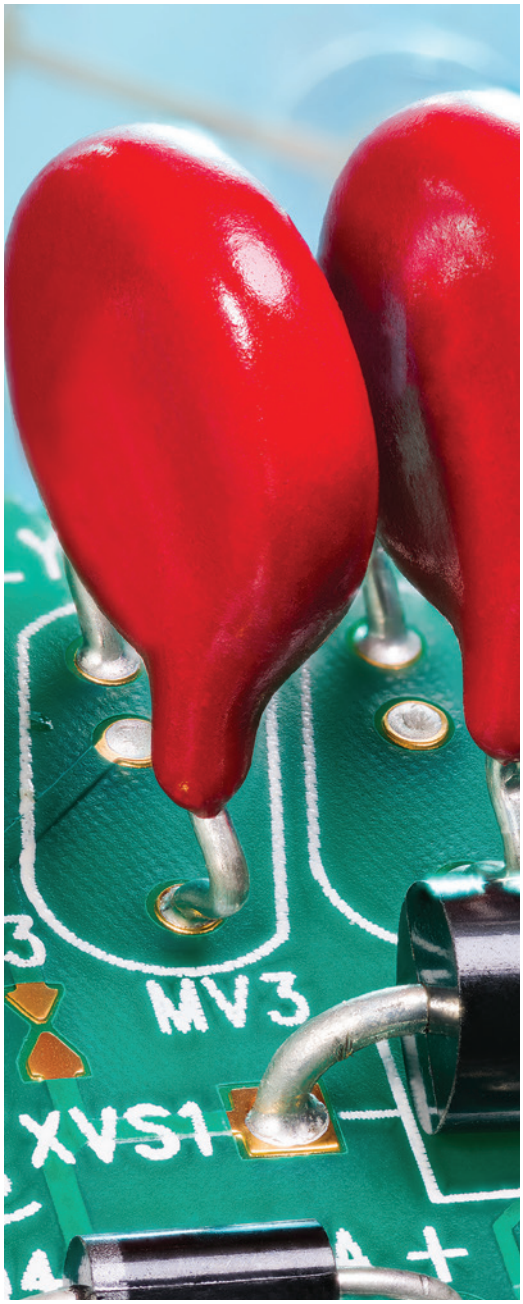
The bottom line? To be safe and to protect yourself or company from liability, be sure you know what the terms mean and follow the standards specific to the industry. If you're not sure, do your homework, ask questions or enlist an expert to help.

ENDNOTES

1. "How Can We Eliminate Static From Operating Rooms to Avoid Accidents with Anaesthetics?," E.I. McKesson, published in the British Journal of Anaesthesia, April 1926. Available at https://academic.oup.com/bja/article/3/4/178/271645.
2. Note that proposed changes in ANSI/ESD STM7.1 would address the need to mitigate the hard line between the conductive and dissipative range.
3. According to FAA-STD-019f, "conductive ESD control materials shall not be used for ESD control work surfaces, tabletop mats, floor mats, flooring, or carpeting where the risk of personnel contact with energized electrical or electronic equipment exists." FAA-STD-019f, Lightning and Surge Protection, Grounding, Bonding, and Shielding Requirements for Facilities and Electronic Equipment, Federal Aviation Administration, published October 18, 2017.
4. "Static electricity and floor resistance," posting to the IBM Knowledge Center website, https://www.ibm.com/support/knowledgecenter/en/SSWLYD/p7eek_staticelectricity_standard.html.

HOW AND WHY VARISTOR FAILURE OCCURS INCLUDING THE EFFECT OF MULTIPULSE SURGES

The Story of the Varistor and the Often-Unappreciated Ways It Can Fail



The year was 2011, and an experiment was being done in China to record the effects of a triggered lightning flash on an overhead transmission line. The line was instrumented to record the induced currents, and the instruments were protected with a metal oxide varistor (MOV).[1] The lightning flash recorded consisted of multiple return strokes, none of which exceeded the Imax rating of the MOV. But, much to the surprise of the experimenters, the MOV was damaged.

How could this happen? And more importantly, why might Imax not be a good basis for selecting an MOV for lightning protection, and are there alternatives? To help answer these questions, we'll discuss in this article what an MOV is and how the way it is made influences its behavior when surged, how failures occur, and how multipulse surges differ from single surges in their effect on MOV properties.

VARISTOR BASICS

In order to understand failure, it's useful to discuss how varistors are made. In this regard, there are three things of note.

First, varistors are a ceramic material composed primarily of zinc oxide (ZnO). At ambient conditions, ZnO crystallizes into a hexagonal wurtzite structure, as shown in Figure 1, where the large balls represent Zn and the small balls represent oxygen (O). This is a complicated structure that, if it crystallized perfectly, would be an insulator. But because the crystallization process isn't perfect, the resulting oxygen vacancies or zinc interstitials cause this structure to become a wide-gap semiconductor having a relatively low resistivity of 1 – 100 Ω-cm at room temperature.

Second, a varistor is not one uniform wurtzite crystal, but many which coalesce into grains. To make ZnO into a varistor, a small amount of Bi_2O_3 is added. The Bi_2O_3 goes into the grain boundaries, as shown in Figure 2. In addition to Bi_2O_3, MnO may be added to enhance the nonlinear

1. A varistor is often called an MOV (Metal Oxide Varistor)

Al Martin holds a BEE degree from Cornell University and a PhD from UCLA. He is the author or co-author of over 35 papers on EMC and telecommunications, and is a Life Senior member of the IEEE and the IEEE SA. Al is also interested in particle physics, and is presently part of a voluntary computing network serving the European Center for Nuclear Research. He can be reached at amartin_36@yahoo.com.

By Albert R. Martin

properties; Sb2O3 to control the ZnO grain growth; and a small amount of Al_2O_3 to increase the ZnO grain conductivity.

The Bi_2O_3 between two ZnO grains results in the formation of back-back Schottky diodes. So essentially, a varistor is a series-parallel arrangement of n-type material separated by back-back Schottky diodes having a voltage drop of about 2V-3V per grain boundary Junction (independent of grain size). According to He [1], this structure can be characterized electrically by Equation (1).

$$I = A_1 exp\left(-\frac{E-mV^{0.5}}{kT}\right) + A_2\left(\frac{V}{V_{th}}\right)^{\alpha} \quad (1)$$

where V is the applied voltage and I is the current through the varistor. Here, E, A_1, A_2, V_{th} and m are constants related to the electrical characteristics of varistor[2], and α is the usual nonlinear coefficient of the varistor. Equation (1) is useful for explaining the shape of the varistor V-I curve.

The first term in Equation (1) is seldom included in the V-I description of a varistor. It is the Schottky emission current in the low current region of the varistor. The second term is the usual nonlinear current in the high current region.

The constants in Equation (1) are controlled by varying the composition of the varistor material and sintering time of the manufacturing process. The threshold voltage V_{th} also depends on composition and sintering conditions. These control the number of grain boundaries between the two electrodes. Since V_{th} is proportional to the number of grain boundaries, more grain boundaries result in a higher V_{th}.

2. E is the excitation energy of varistor, K Boltzmann's constant, A_1, A_2, and m are constants related to the electrical characteristics of varistor, V_{th} is the threshold voltage.

Third, this variation in the varistor fabrication process and the accompanying statistical fluctuations in properties that generally occur in polycrystalline materials cause the resulting varistors to have inhomogeneous electrical properties. That suggests that:

1. The constants in a varistor model like Equation (1) are likely to be different for every varistor; and

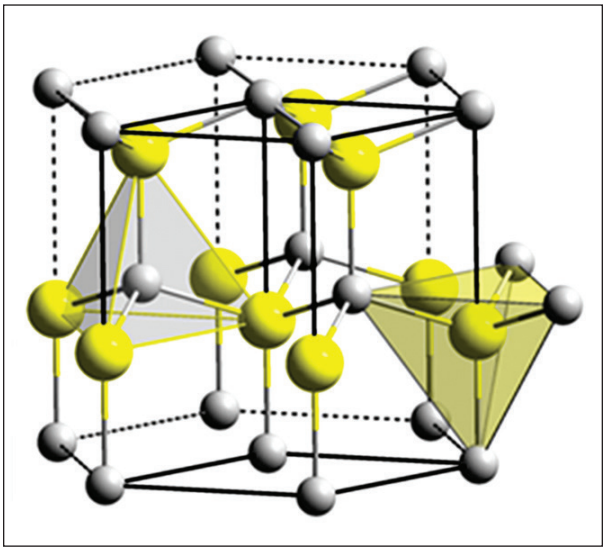


Figure 1: Wurtzite structure. The large balls represent Zn and the smaller balls represent oxygen.

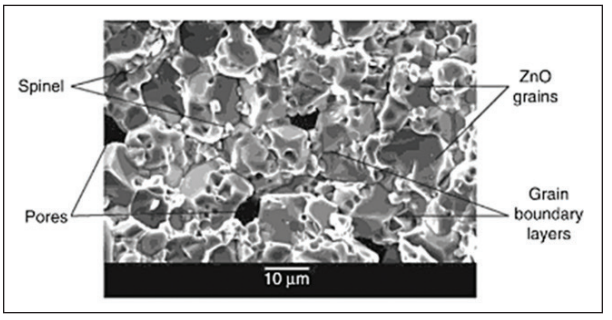


Figure 2: Typical micrograph of varistor structure

2. Not all varistors of the same dimensions have the same properties – an important consideration when choosing a MOV for protection.

VARISTOR FAILURE

Varistors need to absorb the energy deposited by temporary overvoltage, switching surges, or lightning impulses. Experiments show that differences in grain sizes and grain boundary characteristics cause nonuniform microstructure. Nonuniform microstructure results in the variability of varistor current handling capabilities and related energy absorption capability. That, in turn, has a direct relation to failure modes, which include electrical puncture, physical cracking and thermal runaway.

The energy absorption capability can be divided into thermal energy absorption capability and impulse energy absorption capability. Impulse energy absorption capability depends on how the impulse is applied:

- Single impulse stress
- Multiple impulse stress (without sufficient cooling between the impulses)
- Repeated impulse stress (with sufficient cooling between the stresses)

Thermal energy absorption capability, on the other hand, is mainly affected by the heat dissipation capability of the overall arrester design, in addition to the electrical properties of the varistors.

Let's first consider varistor failure caused by heating. At lower currents, the heating localizes in strings of tiny hot spots, which occur at the grain boundaries where the potential is dropped across Schottky-type barriers (see Figure 3). The heat transfer, in this case, is too fast to permit temperature differences that could cause failure.

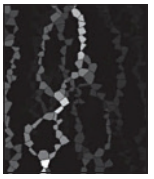


Figure 3: Typical micrograph of grain boundary hot spots

Now consider higher currents. In small varistors (e.g., <25 mm) where the number of ZnO grains between the electrodes might be only about 40, a variation of 3 - 4 grains can cause the current flow in a given path to be an order of magnitude different from surrounding paths. The paths with low breakdown voltages carry most of the current and become hotter, with consequences noted in the study of Sargent *et al* [4]. In that study, analysis of the failed MOV samples showed cracking and a formation of new amorphous material near the conduction channel. Examination of this amorphous material suggested that local hot spots (actually hot channels) were formed when the energy resulting from a current pulse applied to the MOV was absorbed faster than it could be dissipated. The amorphous material in these hot spots likely resulted from a plasma formed during the current pulse. The hot spots rapidly cooled afterward due to heat conduction to the surrounding ZnO grains.

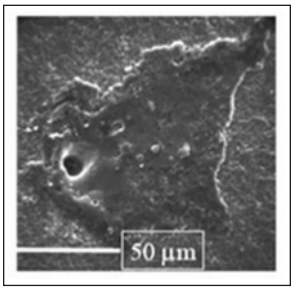


Figure 4: Typical micrograph of a puncture

Under different current conditions, failure modes include electrical puncture (see Figure 4), physical cracking (see Figure 5), and thermal runaway. Cracking happens because varistors are basically a ceramic material,

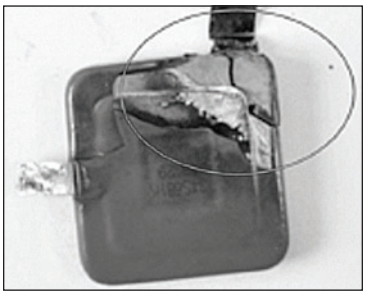


Figure 5: Typical crack formation

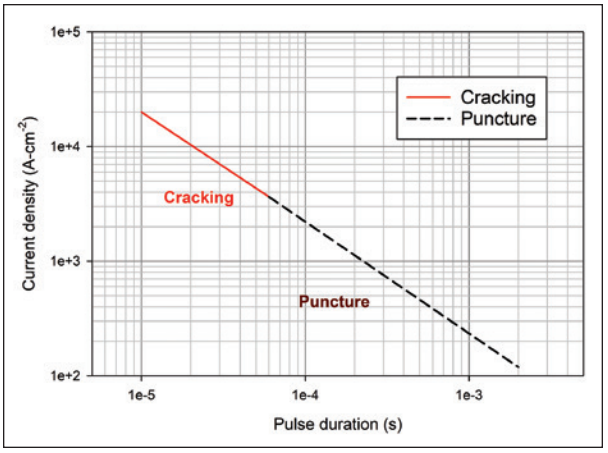


Figure 6: Example of current density and pulse duration combinations that cause failure in varistors. This plot is for a specific varistor. For any other varistor, the scales could be different from those shown.

and hitting them with a sharp high-amplitude surge is like hitting a dinner plate with a hammer.

Puncture destruction occurs in small varistors when the current is relatively low and of long duration (for example, see Figure 6). The net effect is that the varistor heats up. The analysis of a puncture in these varistors strongly indicates that a filament forms with temperatures high enough to melt the Bi_2O_3 (817° C). When this happens, the back-to-back Schottky diodes are destroyed, resulting in reduced filament resistance [1]. Reduced filament resistance permits higher current density, sometimes causing a high enough temperature to melt the ZnO (2000° C).

If the current is continued long enough, the energy deposited in the varistor may raise its temperature to the point of thermal runaway due to the material's negative temperature coefficient of resistivity [1].

Most high impulse currents with short duration can cause a cracking failure (see Figure 5), which typically occurs at the edge of the varistor, since the temperature increases more at the edge of the chip (the white area in Figure 7). The reason is that grain growth during sintering is often more rapid in the outer part of the block than in the center of the block, resulting in fewer and larger grains between the electrodes, and hence a lower breakdown voltage.

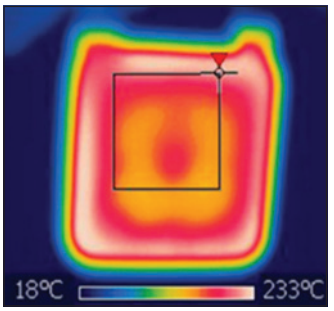


Figure 7: Typical thermal scan of a varistor pulsed under high current

Figure 6 illustrates the conditions under which cracking and puncture can occur. For a given varistor, the red solid line shows cases under which cracking might occur, and the black dashed line cases under which puncture might occur.

FAILURES DUE TO MULTIPULSE LIGHTNING

Why are we talking about muiltipulse lightning? Well, lightning observations and artificially triggered lightning data summarized in [6] show that nearly 70% of cloud-to-ground lightning strokes involve from 2 and up to 26 strikes. These strikes have a geometric mean interstroke interval of about 60 ms. They can also have a long continuing current with an interstroke interval as large as several hundreds of milliseconds. A typical multipulse sequence is illustrated in Figure 8.

Multipulse lightning of the type just described is important because it is capable of producing the temperature rises that lead to the kind of failures just discussed, whereas a single surge might not. For example, in the study by Sargent et al [4], half a set of 18 mm MOV samples were subjected to a multipulse burst of 8/20 surges at rated current. These samples showed signs of damage, whereas the other half of the samples tested with a single 8/20 surge at rated current repeated at intervals of 60 seconds or more showed no damage. In another multipulse burst test, Rousseau et al [7] subjected a MOV to sixty 20 kA 8/20 surges spaced 60 seconds apart, with no failure. But when the same type of MOV was subjected to as few as five 20 kA 8/20 surges spaced 50 ms apart, failure occurred. In these cases, varistor failure was likely caused by heat accumulation due to the relatively long thermal time constant of varistors (Figure 9), illustrated for a single surge using thermal modeling as shown in Figure 10 on page 46 (for details, see [8]).

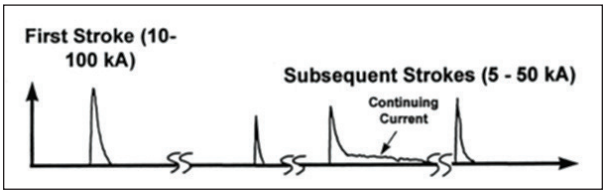


Figure 8: Example of a multipulse lightning flash

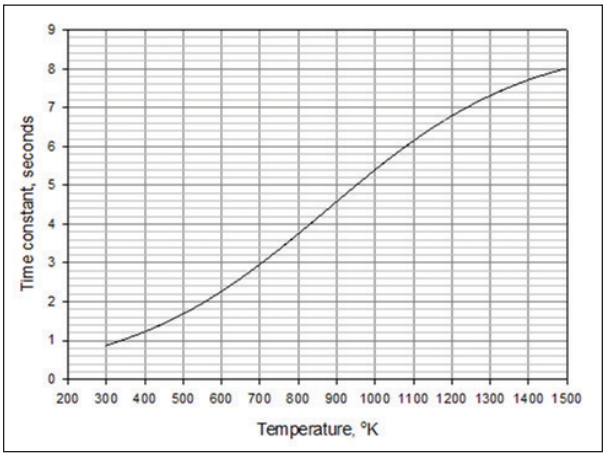


Figure 9: Thermal time constant of a varistor

As noted previously, in the study of Sargent *et al*, analysis of the failed 18 mm MOV samples subjected to a multipulse burst test showed the formation near the conduction channel of a new amorphous material, which was thought to require a local temperature around 1000° C. Thermal modeling suggested that this temperature rise would occur if the pulse power was concentrated in about 2% of the MOV volume. This is an important observation because a calculation of the energy absorbed in the multipulse burst test showed that the temperature rise of the MOV would only have been 231° C if the temperature distribution were uniform, much less than the temperature thought to have caused the damage.

The results of Sargent *et al* suggest that the criterion for failure of an MOV is a localized temperature rise to 1000° C (or the vicinity thereof). So for an MOV under consideration, we need to determine if a localized area might reach 1000° C. Figure 11 shows the additional temperature rise that happens when the surge used to create Figure 10 is applied to the same MOV a second time after 30 ms. The additional temperature rise is due to the relatively long thermal time constant of the MOV, which prevents the MOV from dissipating much heat energy (and hence cooling) before the second surge arrives. The temperature rise is now in the red area above 1000° C, where failure is expected. So this is an example of how a varistor can be destroyed by multipulse surges.

In another look at the effects of multipulse lightning, a study by Zhang *et al* [5] explored the progression of failure in varistors under multiple lightning strokes, using a series of five-pulse groups of 8/20 lightning surges having pulse intervals of 50 ms and pulse amplitudes set at the 20 kA nominal discharge current. The time between the application of one group of impulse currents to a varistor and that of the next group of impulse currents was 30 minutes, allowing a return to the original conditions.

Varistors were judged as having failed when a change greater than ±10% of the original varistor voltage U_{1mA}; the leakage current I_{ie} exceeded 20 μA; or direct damage occurred (typically by edge cracking). The average level change of the U_{1mA} and I_{ie} for the series of impulse groups is shown in Figure 12.

Figure 12 shows that in the absence of continuing current a single multipulse burst didn't deliver enough energy to the MOV to cause failure. Repeated application of the multipulse burst did eventually lead to failure.

So it is possible that a *single* non-destructive multipulse burst conditions the MOV for failure from future multipulse bursts, as suggested by the continually increasing leakage current. This conditioning could be viewed as a kind of accelerated wear-out process.

Microstructural examination of the failed varistors indicated that after the multiple lightning strokes, the grain size decreased and the proportion of Bi in the grain boundary layer increased significantly. These effects were the cumulative result of multiple lightning currents, and were caused by thermal damage and grain boundary structure damage due to temperature

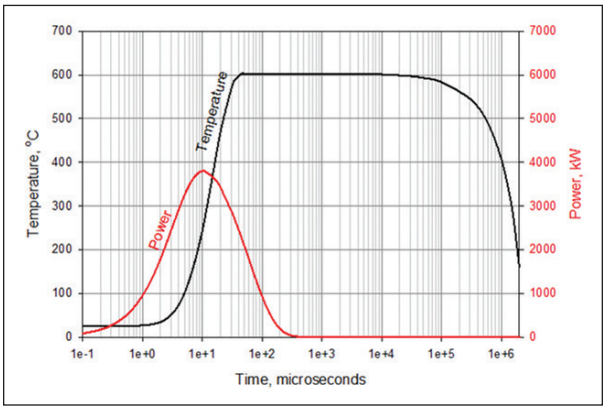


Figure 10: Example of temperature rise in a 25 mm MOV subjected to one 10/63 6 kA surge

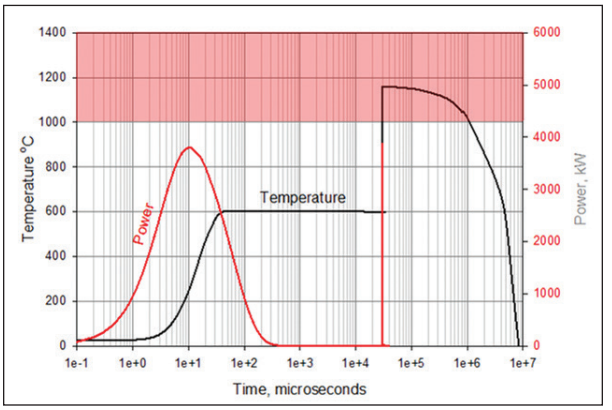


Figure 11: Example of temperature rise for a 25 mm MOV subjected to two 10/63 6 kA surges

gradient thermal stress. This damage eventually led to failure of the MOV. Note that a single surge test would miss this wear-out mechanism.

COMMENTS

It appears that repeated surging of an MOV alters its microstructure, and understanding how that happens is important to understanding how MOVs fail. Which raises some questions. In particular, is the microstructure degradation cumulative as suggested by the current plot in the previous figure? Or are the effects of degradation obscured until it reaches a critical point as suggested by the voltage plot in the previous figure? The answer is likely to depend on the magnitude and spacing of the surges, and there may be a threshold of surge magnitude and surge spacing below which no significant degradation occurs. More research is needed to answer the questions.

High amplitude short-duration single pulse tests (e.g., 6 kV, 3kA 8/20) are typically used to evaluate varistor failure. This type of test may cause a failure mode different from that in a varistor subjected to multipulse lightning at lower amplitude (e.g., cracking vs. wear-out). Single-pulse tests could also miss heat accumulation failures that multipulse lightning can cause, especially multipulse lightning that includes continuing current.

Case in Point

Back to the failure described at the beginning, a triggered lightning flash having multiple return strokes was recorded during a lightning Experiment.

This flash damaged the SPD even though the Imax rating of the SPD (determined by a single surge test) was much higher than the recorded lighting peak current [9]. Why?

As pointed out in [10], what caused failure was the continuing current part of the multipulse sequence, and continuing current is not comprehended in the Imax rating. The continuing current deposited enough energy in the MOV to fail it.

Another Consideration

Since we generally live in a multipulse lightning flash environment, the typical derating plot (created with single surges), as shown in Figure 13, would need to be altered if it is to be used for an MOV that has been installed to protect against multipulse lightning. In particular, the lines in Figure 13 resulting from the (repeated) application of single surges would likely need to be lowered to take into account the microstructural degradation effect suggested by the studies of Zhang *et al* [5].

A multipulse derating plot could be created by repeating Zhang's multipulse group test in the same way as used to create the derating figure Figure 13, but now using multipulse groups instead of single surges. So, for example, for the one-hit line, a group of surges with a relatively narrow waveshape would be applied at a current that would cause failure on the second application. The process would then be repeated using groups of surges with wider waveshapes. The result would be something like the top line in Figure 13.

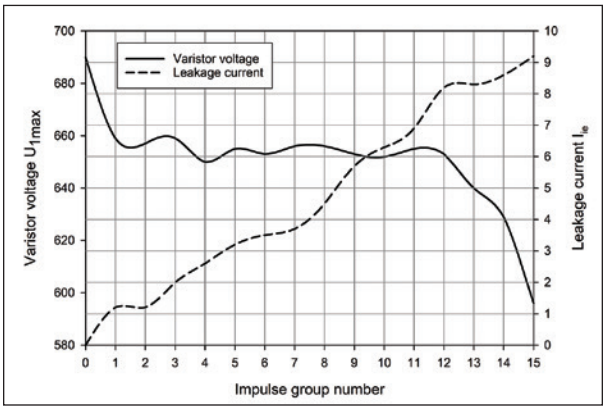


Figure 12: Varistor voltage U_{1mA} and leakage current I_{le} variation of the varistors under multiple lightning impulse current (source: Zhang et al [5])

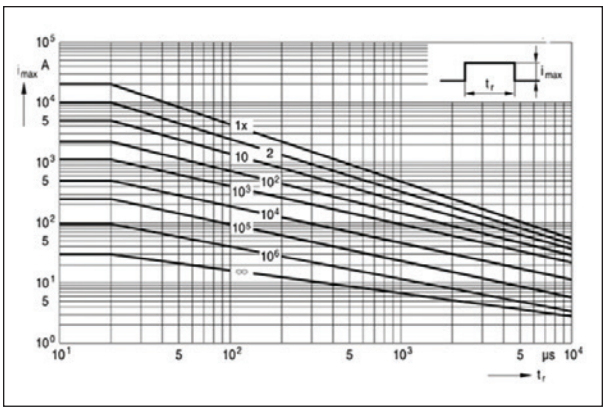


Figure 13: Typical derating curves for an MOV

Similarly, the amplitude of the current would be decreased such that a for the two-hit line, a second group of surges would cause failure on the third application, and the process repeated using groups of surges with wider waveshapes. This process would be continued until enough lines had been generated to adequately characterize the product.

SUMMARY

The varistor fabrication process and the statistical fluctuations in properties that generally occur in polycrystalline materials cause varistors to have inhomogeneous electrical properties. The result is that a few conducting paths with low breakdown voltages to carry most of the current and become hotter. If the temperature of these paths reaches the vicinity of 1000° C, melting occurs and the MOV is destroyed. In the case of 18 mm MOVs, this temperature rise would occur if the inhomogeneities in the MOV cause the pulse power to be concentrated in about 2% of the MOV volume (the 2% may differ in other sizes of MOVs). This temperature rise could be the cause of puncture failure, noted for the case of long-duration lower amplitude surges.

In the case of short-duration high amplitude surges, MOV failure may occur by cracking before melting happens. Single short-duration high amplitude surges might occur on power lines, so MOV ratings established this way can be appropriate for power-line applications

For protection against lightning, ratings established by multipulse testing may be more important. This is because a multipulse lightning surge is often the driver for the temperature rise since it causes energy to accumulate in the MOV due to its long thermal time constant. This is why multipulse testing is important since a single surge test might miss failures that multipulse lightning can cause, notably wear-out, and especially multipulse lightning that includes continuing current. And most lightning is of the multipulse type. The microstructure degradation effect of repeated multipulse surges may need to be considered when constructing derating curves.

Understanding the mechanism of how surging an MOV alters its microstructure is important to understanding how MOVs fail. It is a topic that needs further research.

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October 5-8
MIL-STD-810G: Understanding, Planning and Performing Climatic and Dynamic Testing

October 6-8
ETS-University: Automotive Course

October 12-14
ESD Auditor Certification Course

October 13
Ground Resistance Training Seminar

October 20-21
ETS-University: TILE! Software

October 20-22
Applying Practical EMI Design & Troubleshooting Techniques (Milpitas, CA)

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